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Modeling and Control of a Multi-level Converter for a Photovoltaic Generator Connected to the Grid

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DEDICATION

To my Mother.

Thank you for helping me to flourish. Thank you for accepting me for who I am and where I am at right now. Our family bond is unbreakable and united, we will be able to get through anything. Thank you for creating our strong family unit.

If I could choose anybody at all to be in my corner, backing me up, through all the difficulties of life, it would be my mother a hundred times over. Thank you for always being the most reliable and supportive person I could ever hope to know.

It is not always easy for me to talk about what is going on, but thank you for being there for me. I know I have the strength to handle anything as long as I have the love of my family behind me.

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LIST OF ABBREVIATIONS

PV	Photovoltaic
AC	Alternating Current
DC	Direct Current
MPPT	Maximum Power Point Tracking
PVG	Photovoltaic Generator
FF	Fill Factor
HST	High Speed Train
ICE	Intercity-Express
PWM	Pulse Width Modulation
DAC	Digital-To-Analog Converter
CHB	Cascaded H Bridge
NPC	Neutral Point Clamped
SC	Stacked Cell
FC	Flying Capacitors
SMC	Stacked Multicell Converter

MMC	Modular Multilevel Converter
IGBT	Insulated-Gate Bipolar Transistor
HF	High Frequency
SPWM	Sinusoidal Pulse Width Modulation
SHE	Selective Harmonics Elimination
SVM	Space Vector Modulation
RMS	Root Mean Square
THD	Total Harmonic Distortion
APOD	Alternative Phase Opposition Disposition
POD	Phase Opposition Disposition
PD	Phase Disposition
VFC	Variable Frequency Carrier
MATLAB	Matrix Laboratory
IC	Incremental Conductance
MPP	Maximum Power Point
PQ	Active power/Reactive power
PI	Proportional–Integral
PLL	Phase Lock Loop
VCO	Voltage-Controlled Oscillator
LPF	Low Pass Filter

Abstract

This thesis discusses the employment of multi-level inverters in a grid connected PV system. In this work we carried out the simulation of the grid connected photovoltaic system, with the implementation of multi-level inverters of NPC structure, and with the SPWM as the modulation technique for the control signal generation to the inverter. Dynamic control strategy is essential to use the solar energy efficiently as well as for an energy optimization. We presented a decoupled control of the grid connected PV system using (PI) controller. The decoupled control strategy allows the control of the real power (*P*) and the reactive power (*Q*) independently, and with the utilization of the incremental conductance MPPT.

Key words: Multi-level inverters, grid connected PV system, incremental conductance MPPT, PQ control.

Resumé

Cette thèse traite de l'utilisation d'onduleurs à plusieurs niveaux dans un système PV connecté au réseau. Dans ce travail, nous avons effectué la simulation du système photovoltaïque connecté au réseau, avec la mise en œuvre d'onduleurs multi-niveaux de structure NPC, et avec le SPWM comme technique de modulation pour la génération du signal de commande vers l'onduleur. Une stratégie de contrôle dynamique est essentielle pour utiliser efficacement l'énergie solaire ainsi que pour une optimisation énergétique. Nous avons présenté un contrôle découplé du système PV connecté au réseau à l'aide d'un contrôleur (PI). La stratégie de contrôle découplé permet le contrôle de la puissance réelle (P) et de la puissance réactive (Q) indépendamment, et avec l'utilisation de la conductance incrémentale MPPT.

Mots clés: Onduleurs multi-niveaux, système PV connecté au réseau, conductance incrémentale MPPT, contrôle PQ.

الملخص

تناقش هذه الرسالة توظيف محولات متعددة المستويات في نظام كهروضوئي متصل بالشبكة. في هذا العمل نفذنا محاكاة كتقنية SPWM ، وباستخدام NPC النظام الكهروضوئي المتصل بالشبكة ، مع تنفيذ محولات متعددة المستويات لهيكل تعديل لتوليد إشارة التحكم إلى العاكس. استراتيجية التحكم الديناميكي ضرورية لاستخدام الطاقة الشمسية بكفاءة وكذلك تسمح .(PI) لتحسين الطاقة. قدمنا عنصر تحكم منفصل عن النظام الكهروضوئي المتصل بالشبكة باستخدام جهاز التحكم بشكل مستقل ، وباستخدام التوصيل (Q) والقوة التفاعلية (P) إستراتيجية التحكم المنفصلة بالتحكم في القدرة الحقيقية الإضافي MPPT.

الكلمات المفتاحية: تحكم MPPT, محولات متعددة المستويات ، نظام كهروضوئي متصل بالشبكة ، توصيل تدريجيPQ

General Introduction

With the increasing concern about global warming, the necessity to generate pollution-free power is a must. The photovoltaic PV generation system is one of the best renewable energy sources available to meet out the energy crisis. It is safe, pollution free, and it necessitates less maintenance and inexhaustible. The standalone PV system is commonly employed in remote places where the power generation is needed. The 3-phase system connected to the distribution network is therefore seen as cost savings for investment. The PV array is linked to the utility grid with an inverter. To keep the standards for THD, grid current controls and grid synchronization during normal / defective conditions is essential.

The incorporation of renewable energy sources with the grid plays a vigorous role in energy utilization. It is difficult to use the power from renewable energy sources directly for the injection into the distribution network. Therefore, the system needs power converters as a crossing point between renewable energy sources and grid/load.

As part of the research into harmonic reduction methods, several works have been conducted on two axes. The use of multilevel topologies for the inverter, also the control of the opening and closing of the switches forming the inverter.

Using modulation techniques as a control strategy for controlling the opening and closing of the switches dramatically reduces harmonics.

Sinusoidal modulation seems the best technique for controlling the opening and closing of switches, but it requires knowledge of the switching times at each modulation moment, in addition the control of the switches of each arm of the inverter must be done d 'a separate way. The system studied in our work consists of a multi-level inverter of the NPC type controlled by sinusoidal PWM.

The work presented consists of chapters:

The first chapter we review the general system structure as well as the analysis of the constituents of the grid connected PV system.

In the second chapter we dealt with the detailed study of the NPC type three-level inverter, and the modeling of the constituents of the system.

The third chapter was devoted for the main control methods of the components of the system, we will start off by explaining the modulation strategy of the multi-

level inverter for the generation of the control signals for the switches. In the second part of this chapter we will focus on the maximum power point tracking for the PV array.

In the fourth and last chapter of the study, we presented the simulation results of the 100kv grid connected PV systemachieved with the use of MATLAB/Simulink environment.

State of the art of the PV system connected to the grid

Chapter outline

1. Introduction

Renewable sources of energy have received increasing attention worldwide as a result of environmental and CO_2 emission issues. Several countries have set an ambitious goal for renewable energy production potential.

In relation to the timeline, Algeria's renewable energy goals are optimistic. Algeria will need an additional 5000 MW to attain the solar capacity goal outlined in the regulator's 2028 generation capacity scenario. with approximately 450 MW of solar power today. 22 000 MW gross renewable capacity will have to be deployed to achieve the official 2030 goals [Eng].

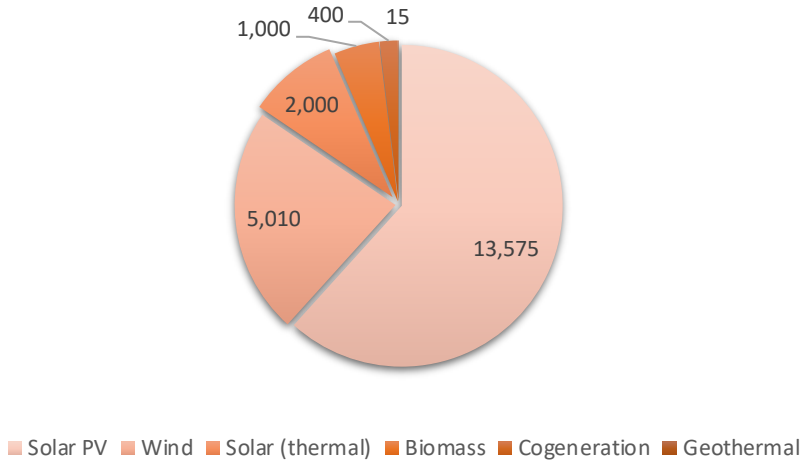


Figure 1.1 2030 targeted renewable energy mix. (MW) [S.y]

Among other renewable energy sources, photovoltaic (PV) systems have a potential to become a main source of electricity in the nearby future because of numerous merits such as simple installation, modularity, and scalability. In fact, the installation and component cost of PV systems, the price of the PV panel, in particular, have decreased significantly in recent years. This has resulted to increasing installation and connection of PV systems in the past years with the electricity grid. However, the incorporation of PV systems into the power grid becomes essential in the broad adoption of grid linked PV systems. In practice, a high penetration rate of the grid linked PV system has seen challenges such as overload of the network during peaking power generation times, extreme grid power fluctuations due to PV interference and the reduced capacity for regulating grid frequencies due to more decentralized power generation units.

2. Structures of the PV system connected to the grid

A general system structure of grid-connected PV systems is shown in Fig. 1.2[1] and consists of three main components: PV panels (or arrays), power converters (PV inverters), and AC grid. As the power generated by the PV arrays is DC power, the power converter, which is a power electronic-based technology, is required to convert the DC power from the PV arrays to the AC power [1].

In other words, power converter plays an important role in controlling the power delivery and at the same time ensuring a proper integration between the PV and the grid. Additionally, other specifications are imposed by the grid requirements to make grid-connected PV systems more resilient and grid-friendly: 1- reliable or secure the power supply; 2- flexible control of active and reactive power; 3- dynamic grid support per demands; 4- system condition monitoring, protection, and communication; and 5- high efficiency and reliability, low cost, and small volume [2, 3].

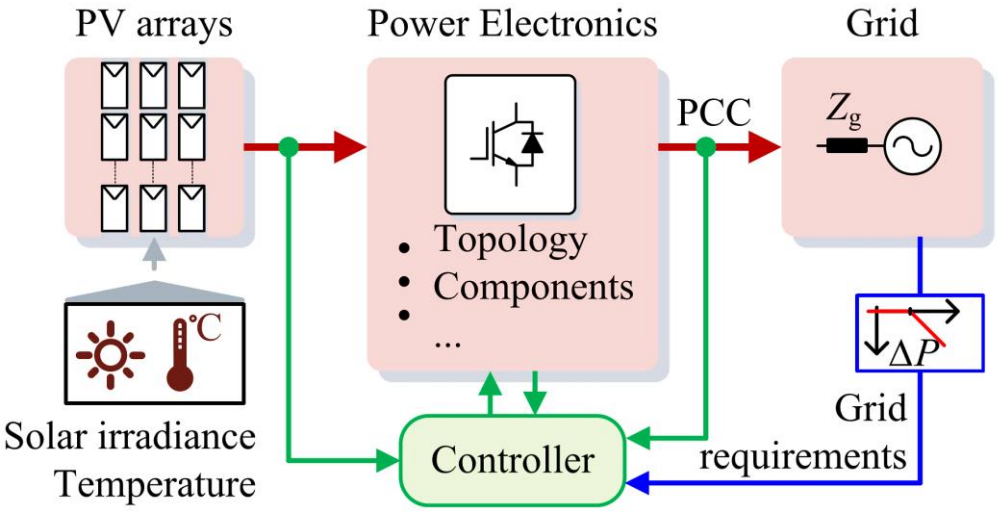


Figure 1.2 General system structure of the grid-connected photovoltaic (PV) system [4].

In the state-of-the art technology, there are three mainstream system configurations of grid-connected PV systems, as summarized in Fig 1.3 [4, 5] The adaptation of each configuration is mainly dependent on the applications and the power ratings. For example, a small-scale PV system usually employs module

[1] the PV arrays are the source of input power and power converters are employed to enable the control of the PV systemand the integration of the grid, whose control strategy is imposed by the grid requirements.

PV converters shown in Fig. 1.2(a)[2] because of the small volume and high scalability. The module PV converter enables individual MPPT tracking at each PV panel, which is the advantage of this configuration due to the increased energy yield.

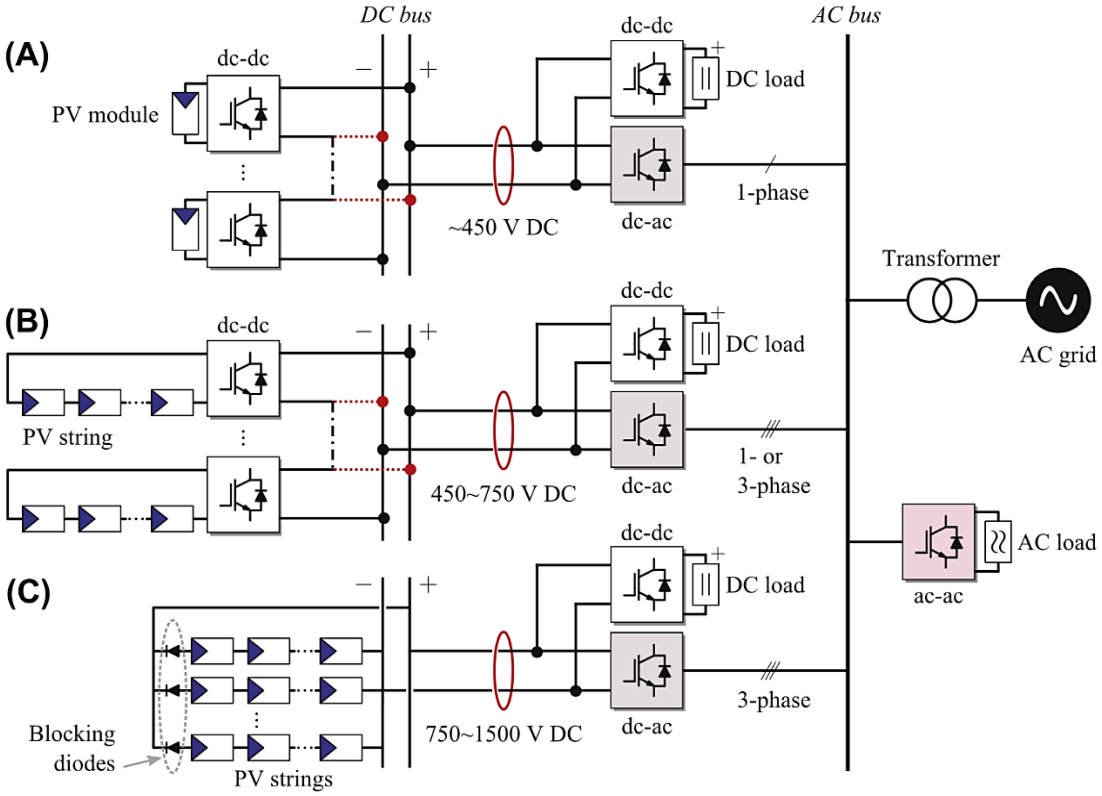


Figure 1.3 Different grid-connected photovoltaic inverter structures [5].

Nevertheless, this configuration requires a DC-DC converter with high conversion ratio, as the PV voltage of the module is usually small because of the limited number of panels, to be able to be connected to the AC grid through the inverter. At the same time, high efficiency needs to be attained over a wide range of operation, which is a challenge of this system configuration. For a medium/large-scale PV system, string, multistring, or central inverters shown in Fig. 1.2(b)[3] and C[4] are more promising because of their overall high conversion efficiency. In this case, the PV power can be directly fed to the AC grid without

[2] (A) module inverters connected to a common dc-bus.

[3] (B) string/multistring inverter applied in single- or three-phase systems (residential and commercial applications).

[4] (C) center inverters for commercial or utility-scale applications (high power, e.g., 100 kW).

or with a DC-DC converter with a small conversion ratio, as the PV voltage is usually high enough because of the large number of PV panels. As the PV utilization is still at a residential application (e.g., rooftop system), the string and multistring inverters are dominating in market, and the single-phase connection is more often to see [6].

Admittedly, because of its high scalability, great reliability and easy installation the string inverter is becoming more and more widespread. In the particularly large PV systems this system arrangement should be utilized to replace the central inverter. The number of power transfer stages used on the system can also be considered to categorize the PV system structure.

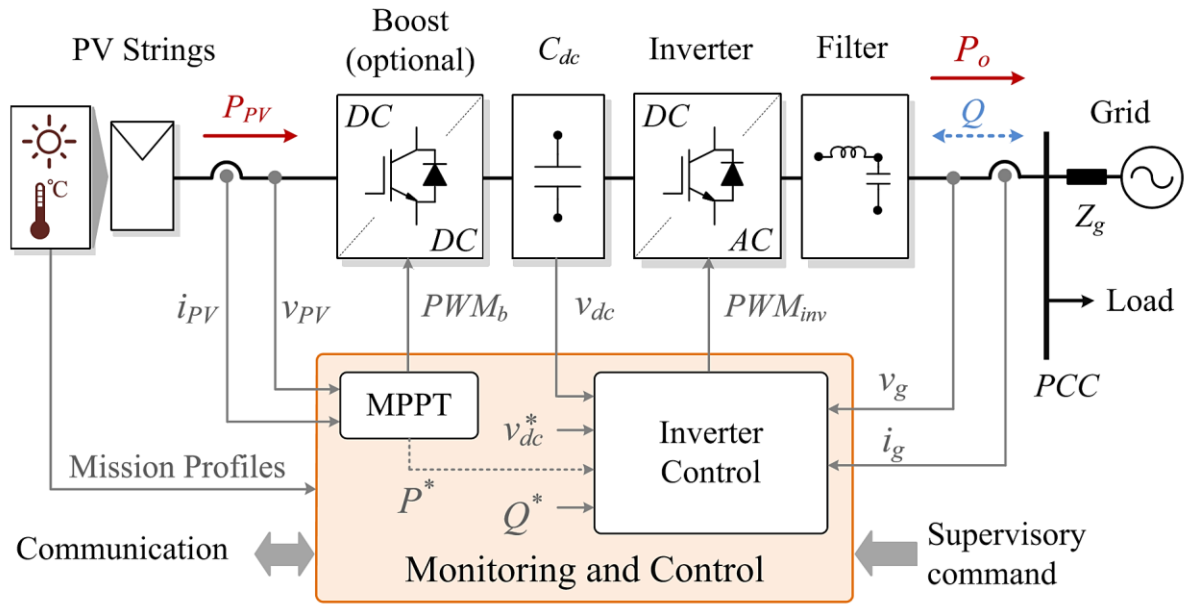


Figure 1.4 System configuration of a two-stage, single-phase, grid-connected photovoltaic system [5].

The PV-power voltage is typically smaller than the necessary DC-link voltage for a small-scale (for example, modular converter, string/multi-string inverter) Due to the small number of connected PV panels in succession. In this case, it is usually necessary to convert two stages of electricity. The first phase of conversion is a conversion DC-DC that increases PV voltage so as to meet the necessary minimum DC link voltage for grid connected applications. The PV voltage is normally sufficient to link to the grid without increasing the voltage for a large photovoltaic module. In this chapter, the single-phase string inverter configuration is used as an example as a result of its popularity. An example of the two-stage grid-connected PV system with an LCL filter is shown in Fig. 1.4. Moreover, to achieve a higher efficiency, transformer-less PV inverter topologies are favorable. However, the lack of isolation transformers can compromise the

safety of the system because of the generated leakage currents, which may need to be addressed by specifically designing the modulation schemes or bypassing methods [7, 8].

3. Analysis of the constituents of PV system connected to the grid

3.1. The photovoltaic solar cell

3.1.1. definition

The fundamental building block that converts solar rays into electrical energy in a photovoltaic system is the photovoltaic solar cell demonstrated in Fig. 1.5. It consists of a PN junction of a semiconductor material (usually silicon).

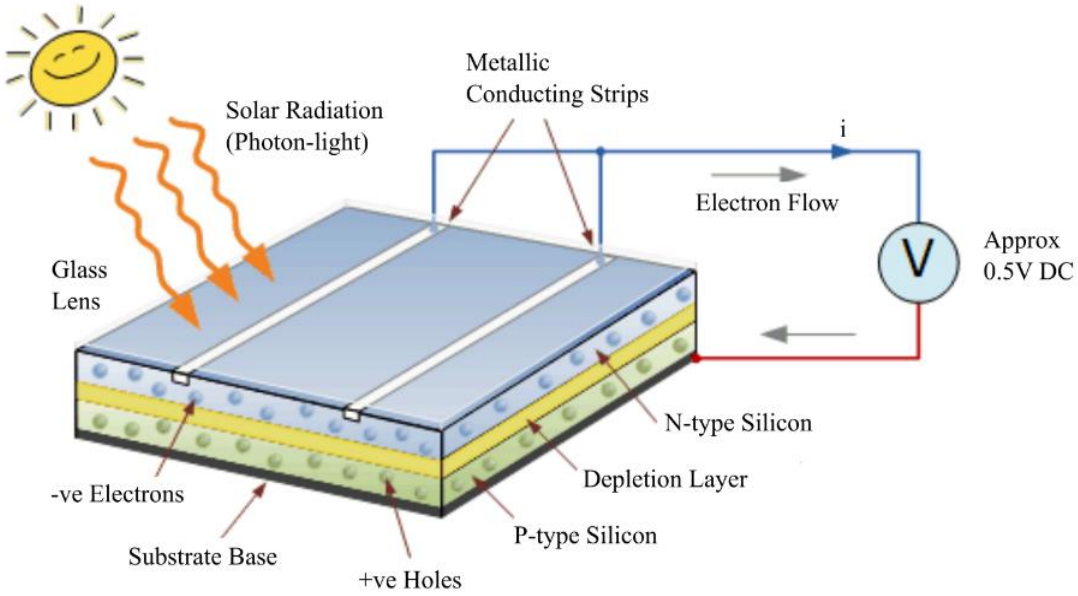


Figure 1.5 Description of the photovoltaic cell [10].

A PV (or PV panel) module consists of assembling a number of serial / parallel PV cells connected to supply the voltage and current required. All the modules mounted in series / parallel form a photovoltaic field [9]. The PVG can be either fabricated of a single PV module, or of the association of several PV modules. In the case of a so-called "string" system (see Fig. 1.3), the PVG consists of strings connected in parallel or in series to which a "bypass" protection diode is attached.

3.1.2. Modeling of the solar cell

Ideally, a PV cell is modeled by a current generator with a diode in parallel. In this configuration, the current injected by the source is representative of the energetic sunshine (also called irradiance) and of the PV cell surface. The current-voltage property $I(V)$ of the diode is non-linear and gives a fairly accurate account of the $I(V)$ behavior of the cells.

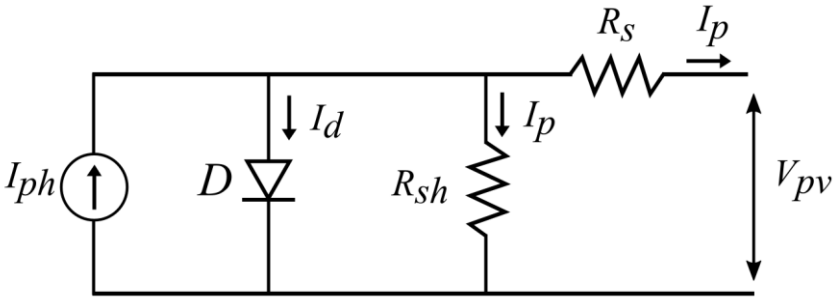


Figure 1.6 Equivalent diagram of a PV cell. [S.y]

Two resistors are added to the model. One in series (R_S) and the other in parallel (R_{Sh}). Resistance R_S characterizes the voltage drops due to the connection contacts between the different cells while resistance R_{Sh} characterizes the leakage current in the diode [10]. The equivalent electrical model of a PV cell is given in Fig. 1.6.

The mathematical model which governs the diagram of Fig. 1.6 is indicated in the equation Eq. 1.1.

$$I_{pv} = I_{ph} - I_S\left(e^{\frac{Q(V_{pv}+R_S.I_{pv})}{n.K.T}} - 1\right) - \frac{V_{pv} + R_S.I_{pv}}{R_{Sh}} \qquad \text{(Eq.1.1)}$$

I_{ph} : the photocurrent (A)

I_{pv} : Current delivered by the cell (A)

V_{pv}: Voltage generated by the cell (V)

I_S: Diode saturation current (A)

T: Cell temperature (K)

n: Cell ideality factor (n between 1 and 2)

K: Boltzmann constant, $K = 1.38 \times 10^{-23}\ (J/K)$

Q: Charge of an electron, $Q = 1.16 \times 10^{-19}\ (C)$

The current-voltage $I\ (V)$ and power-voltage $P\ (V)$ characteristic curves of PV cell obtained from equation Eq. 1.1 are shown in Fig. 1.7.

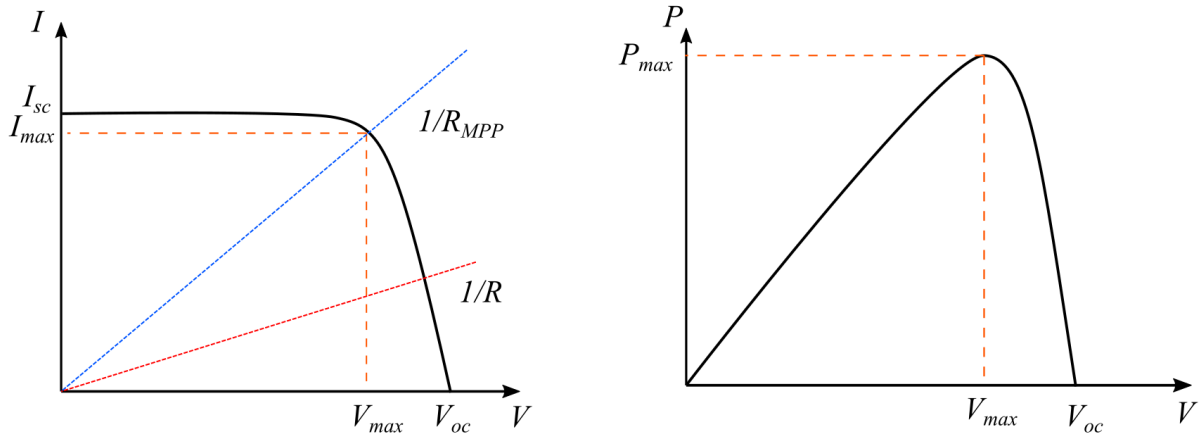


Figure 1.7 I (V) and P (V) characteristic curves of a PV cell. [S.y]

Thus, the mathematical model of the PV modulus can be obtained by considering the following equations : [9]

$$I_{mpv} = N_p \times I_{pv} \qquad \text{(Eq.1.2)}$$

$$V_{mpv} = N_S \times V_{pv} \qquad \text{(Eq.1.3)}$$

I_{mpv} : PV module current (A)

V_{mpv} : PV module voltage (V)

N_S : Number of PV cells connected in series.

N_p : Number of PV cells connected in parallel.

3.1.3 The conversion efficiency of a solar cell

Now, we are able to determine the conversion efficiency of the solar cell. It is defined as:

$$\eta_{max} = \frac{P_{max}}{P_{in}} = \frac{V_{max} \cdot I_{max}}{P_{in}} \qquad \text{(Eq.1.4)}$$

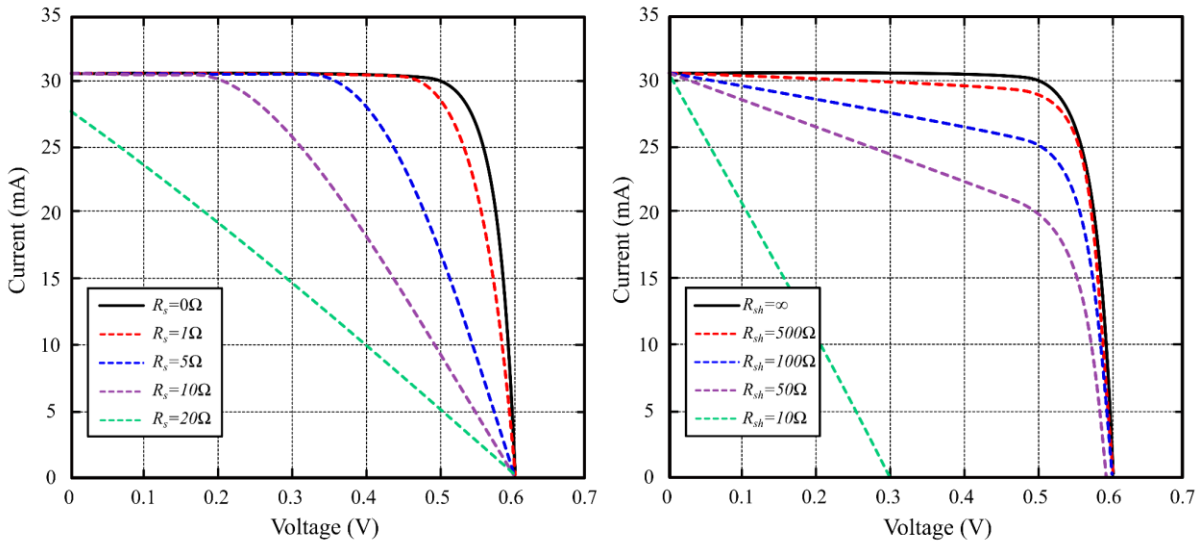
where P_{in} is the incident solar power, for 100 mW/cm^2. We also define the fill factor (FF) of the $I-V$ curve as

$$FF = \frac{V_{max} \cdot I_{max}}{V_{oc} \cdot I_{sc}} \qquad \text{(Eq.1.5)}$$

It is a measure of the squareness of the $I-V$ curve. As FF increases, the efficiency increases. The solar cell designers try also to maximize the FF. It increases by lowering Is and R_S and increasing R_{Sh}.

Assuming $n = 1$, $R_S = 0$, $R_{sh} = \infty$, $I_{ph} = 30.4\,mA$, $I_s = 1.66 \times 10^{-12}\,A$. For this example, the open circuit voltage amounts to $0.605\,V$ for c-Si-cells. The effect of R_S on the $I-V$ curve of a solar cell is depicted in Fig. 1.8(a) (taking $R_{sh} = \infty$). We see from this figure that as R_S increases, the short circuit current begins to decrease first at high values of the series resistance, while the open circuit voltage remains constant. The maximum output power decreases because of the power consumption in R_S. So, R_S must be minimized.

Additionally, Fig. 1.8(b) shows the effect of R_{sh} on the $I-V$ curve of a solar cell (taking $R_S = 0$). We see from this figure that V_{oc} and the output power decrease because of the power loss in R_{sh}. So, R_{sh} must be increased to the highest suitable value.



(a): Effect of R_s on the I-V solar cell characteristics. (b): Effect of R_{sh} on the I-V solar cell characteristics.

Figure 1.8 Effect of R_S & R_{sh} on the I-V solar cell characteristics. [S.y]

As the solar cells are subjected to the environment where the temperature varies in a wide range, the effect of temperature on a solar cell performance must be considered.

3.2. Static converters for grid connected PV systems

The adaptation and conversion of the DC power obtained by the PVG into AC power adapted to that of the network are ensured by the static converters which are the DC-DC converters (choppers) and the DC-AC converters (inverters).

3.2.1. Static converters DC-DC

A static converter DC-DC is an energy converter which converts a fixed DC voltage (or current) into a variable DC voltage (or current).

Considering our application (PV system), we are mainly interested in the step-up voltage converter (Boost). Indeed, in a photovoltaic system of small and medium power, often, the voltage delivered by the photovoltaic generator (PVG) is lower than the necessary input voltage of the inverter. It is therefore necessary to rise the voltage supplied by the PVG. This is the main role of the Boost converter.

In the literature, the Boost chopper itself is divided into four main structures [11] as shown in Fig. 1.9.

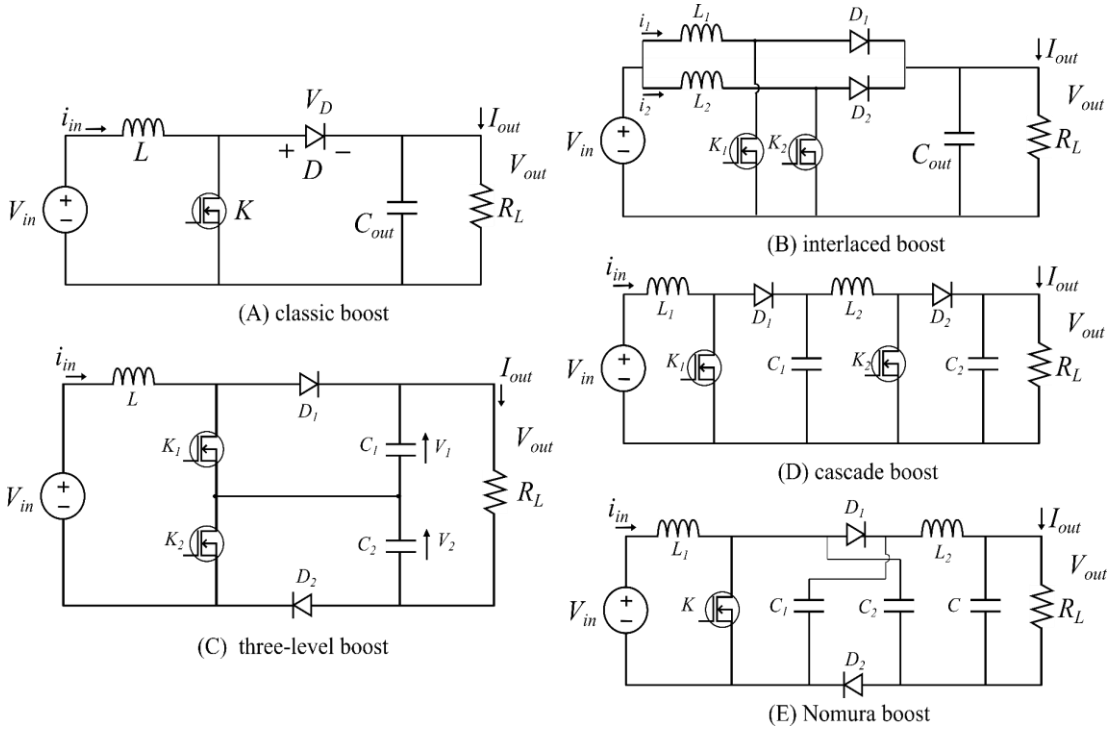


Figure 1.9 Different topologies of the Boost converter. [S.y]

In fact, when the input current is greater (case of a PV source formed by several panels in parallel or a fuel cell source), it may be necessary to segment the input current by putting two or more elementary cells in parallel (Fig. 1.9(b)). This allows it to reduce the current constraints for the switches (transistors and diodes)

forming the structure of the converter. The tension stresses can also be reduced by placing two or more elementary cells in series (Fig. 1.9(c)).

3.2.1.1 Classic boost

The classic boost converter is displayed in Fig. 1.9(a). The advantage of this converter is that it is easy to control compared to other structures given the number of components involved.

But if the power is increased, this arrangement has major drawbacks, voltage and current constraints as well as high input current and output voltage ripples at the switching frequency. Indeed, in the "OFF" state, the switch must block the full output voltage which is too high and in the "ON" state it must also withstand the entire input current. These two conditions will influence the price of electronic components and therefore the converter's cost [11].

3.2.1.2 Interlaced boost

Interlaced Boost is used nowadays in several so-called low voltage / high current application areas. For example, applications VRM (Voltage Regulator Module) which provides power to microprocessor cards and their peripherals. Medium and high power applications such as the uninterruptible power supply (ASI) backup system also use this type of converter. The same is true for applications dedicated to on-board energies (electric and hybrid vehicle, avionics, naval etc.) [12]

The structure of this type of converter is formed by the parallel association of two or more elementary cells. This paralleling makes it possible to share the current between the different cells. In the case where two cells are put in parallel, the diagram of the interlaced Boost is given in Fig. 1.9(b). In this structure, each elementary cell is controlled with the same duty cycle α and the controls are shifted by a time equal to the chopping period divided by the number of switching cells (q). In this situation, the current passing through each cell is divided by (q).

The current stresses undergone by the switches are thus reduced. Another advantage of this arrangement is the reduction in the ripple of the input current. In fact, placing q elementary cells in parallel multiplies by q the apparent frequency of the switching harmonics of the input and output current (see Eq. 1.7). This makes it possible to reduce the volume of filtering and thus miniaturize the output converter-filter assembly. This also makes it possible, on the one hand, to improve the dynamics of the converter (especially since we can even choose MOSFETS and take advantage of their speed performance) and to reduce the overall cost of manufacturing the Boost converter from somewhere else.

However, this structure has the drawback because to the number of components used for the manufacture of the converter and the problem of balancing the currents flowing through the different elementary cells.

3.2.1.3 Three-level boost

The three-stage boost is shown in Fig.1.9(c), This converter uses a single inductor but two controlled switches, two diodes and two capacitors [13]. The advantage of this assembly is to halve the voltage constraints of the switches. These switches are, as in Interlaced Boost, controlled by the same duty cycle but their controls are offset by half a period. This converter can also double the apparent frequency response of the input current, leading to a decreased ripple of the input current with the same inductance. The current transistor and diodes constraints are comparable with those of a traditional Boost and the semi-conduction component's voltage constraints are reduced in half.

Note: the author [11] indicates that the previous three structures (Classic Boost, Interlaced Boost, and Three Voltage Level Boost) have the same voltage ratio shown in Equation Eq. 1.6.

$$\frac{V_S}{V_e} = \frac{1}{1-\alpha} \qquad \text{(Eq.1.6)}$$

Where: V_e is the input voltage of the converter, V_S is the output voltage and α is the duty cycle of the drive.

3.2.1.4 Cascade Boost

This converter's block diagram is displayed in Fig. 1.9(d). This converter is obtained by the cascade association of two identical elementary Boosts. It has the advantage of a very high tension ratio compared to previous structures but has the disadvantage of the difficulty of control due to the increased order of the system [27]. The voltage ratio of this converter is shown in equation Eq. 1.7.

$$\frac{V_S}{V_e} = \frac{1}{1-\alpha_1} \times \frac{1}{1-\alpha_2} \qquad \text{(Eq.1.7)}$$

With: α_1 is the duty cycle of the control of switch 1 and α_2 is that of switch 2.

3.2.1.5 Nomura boost (high voltage gain)

The schematic of this converter is showed in Fig. 1.9(e). Nomura Boost (also known as High Voltage Gain Boost) has the advantage of achieving a high voltage ratio with a single controlled switch. But it uses two identical capacitors

connected through two diodes. The current constraints on the switch are greater than those of the classic Boost. In contrast, the stresses on the diodes is lower than the classic Boost. The voltage ratio of this converter is given in equation Eq. 1.8.

$$\frac{V_S}{V_e} = \frac{1+\alpha}{1-\alpha} \qquad \text{(Eq.1.8)}$$

3.2.2 Static converters DC-AC

An inverter is a static converter of power electronics which converts a direct voltage (or current) DC into an alternating voltage (or current) AC. There are mainly two types of voltage inverters connected to the grid depending on the power level to be injected: the single-phase inverter and the three-phase inverter [14].

a. The single phase PV inverter connected to the grid

Single phase PV inverter topology is widely used in commercial PV inverters [14]. The power range of the single-phase photovoltaic inverter is generally between 2.2 kW and 6 Kw. The advantage of the system PV with single-phase inverters lies in the simplicity of its topology and the investment cost, but it is limited in terms of transmitted power and its control is quite complex due to the difficulty resulting from information fields more reduced.

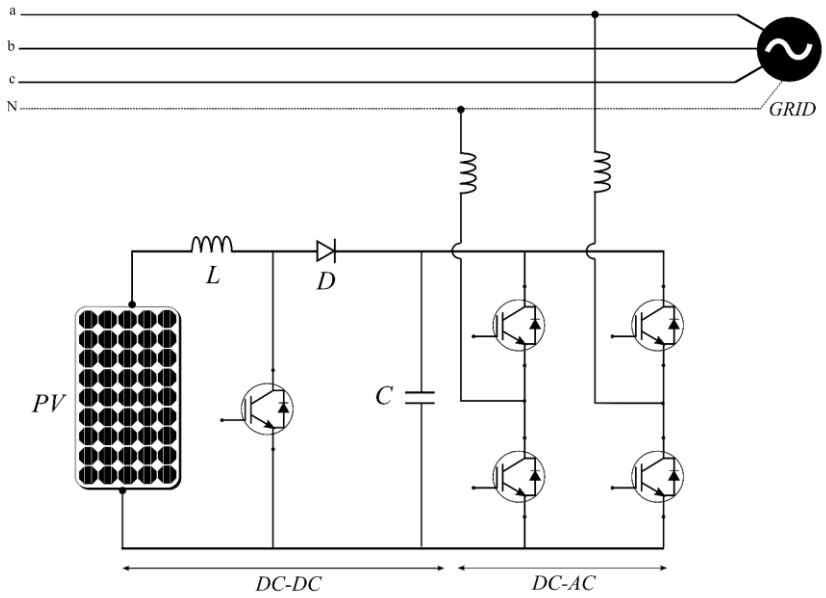


Figure 1.10 Single phase PV inverter connected to the grid. [S.y]

b. Grid Connected Three-Phase PV Inverter Topologies

The three phase PV system connected to the grid is able to produce more power compared to the single phase PV system.

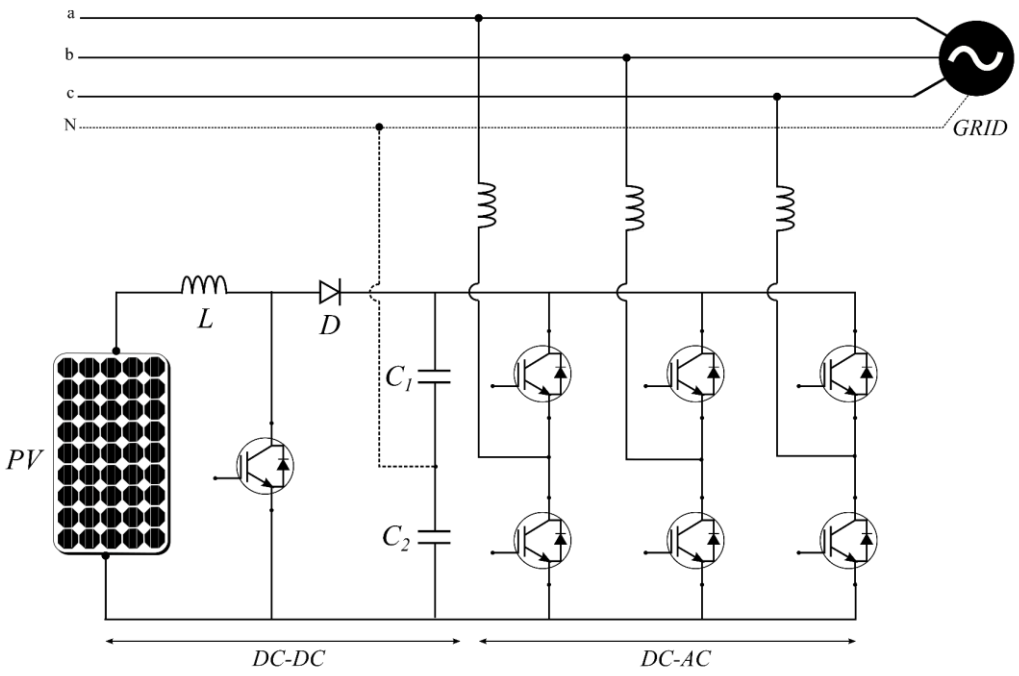


Figure 1.11 Three phase PV inverter connected to the grid. [S.y]

Whether single-phase or three-phase, voltage inverters can be categorized into two groups: the classic inverter (with 2 levels) and the multicellular inverter (multi-level) when a phase is made by the link of several switching cells. Multicellular inverters are categorized into multicellular "series" or "parallel", depending on whether the switching cells are associated in series or in parallel.

Fig. 1.12 shows a flowchart for classifying inverters. This non-exhaustive diagram shows the main inverters that exist in the literature. There are also other subcategories that we will not discuss in this manuscript.

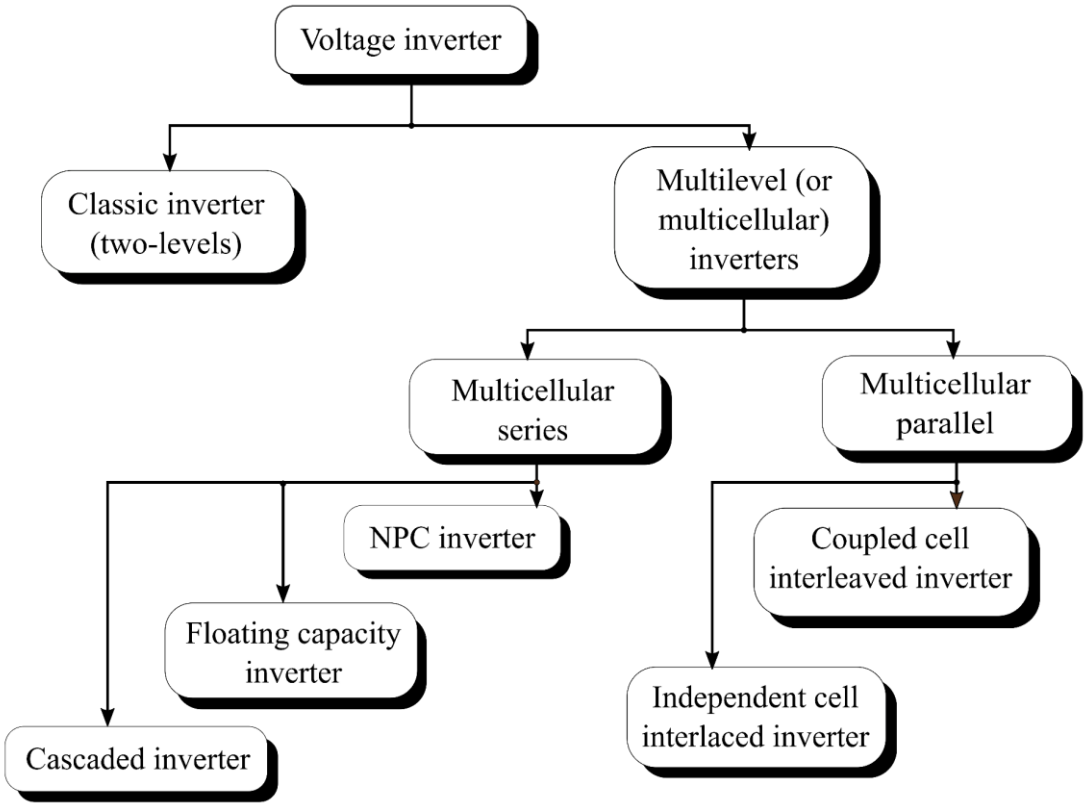


Figure 1.12 Different inverter topologies. [S.y]

3.2.2.1 Classic inverter (two-levels)

The classic inverter has been shown previously in Fig. 1.11 The advantage of this converter lies in the simplicity of its structure. However, it has the drawback of being limited in high power. It is for this reason that this structure is used in: HST (High speed train) by Alstom; ICE (Intercity-express) by Siemens and in almost all electric vehicles. In addition, an output filter must be associated with it, the passive components of which must be specifically sized (in addition to the filtering constraint) to obtain good system efficiency (low losses in the inductive components). This constraint increases the volume of the filter and decreases the dynamics of the system. To increase this dynamic, small passive components (L, C) can be used, but in this case, the efficiency of the system is degraded because of the increase in current ripples flowing through the inductors of the filter. Consequently, there is a compromise between the dynamics and the efficiency of the system. The conventional inverter is usually controlled by an intersective or vector PWM control.

3.2.2.2 Multi-level inverters

a. Multilevel concept

A static converter is said to be "multilevel" when it generates a chopped output voltage composed of at least three levels. This type of converters has two main advantages. On the one hand, the multilevel structures make it possible to limit the voltage stresses undergone by the power switches. Each component, when in an OFF state, withstands a percentage of the full DC bus voltage as the number of levels increases. Also, the output voltage delivered by multilevel converters has interesting spectral qualities. Multiplying the number of intermediate levels reduces the amplitude of each rising or falling edge of the output voltage [15]. The harmonic lines therefore have reduced amplitude. In the specific case of PWM operation, the use of a multilevel converter combined with judicious control of the power components also makes it possible to eliminate certain groups of harmonic lines.

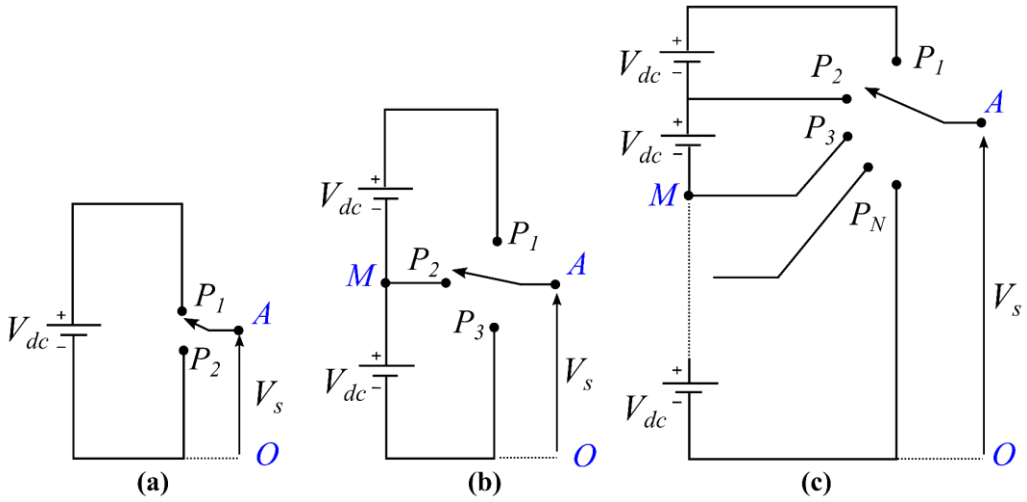


Figure 1.13 Diagram of an inverter arm with two levels (a), three levels (b), N levels (c). [S.y]

The inverter in Fig. 1.13(a) delivers two voltage levels at its output:

- Position P1: $V_S = V_{dc}$
- Position P2: $V_S = 0$

The three positions P1, P2, P3 of the switch in Fig. 1.13(b), allow to have respectively three voltage levels ($2V_{dc}$, V_{dc} and 0). Hence the name three-level inverter. The generalization of this principle makes it possible to obtain the N-level structure of the Fig. 1.13(c).

The increase in the numbers of DC sources and hence in the levels undoubtedly leads to a minimum of harmonics for the voltage form at the output of the converter.

b. Multilevel Conversion History

The first traces revealed on multilevel converters date back to the 1960s, 1962 to be precise, when [16] puts in series, via a transformer, several phase-shifted inverters between them. Then, [17] transposes the concept of the digital-to-analog converter (DAC) for power electronics by multiplying the number of potentials available in order to minimize the difference between the output signal and the sinusoidal reference (signal in steps of staircase). The point here is to reduce the annoying harmonics of a "full wave" inverter (offering square signals) at 2 levels. In 1971, the “H-bridge” (single-phase inverter with 3 voltage levels) was put into series (cascade) by [18], offering both fewer harmonics and sizing of the active components inversely proportional to the number of levels, and referred to as "Cascaded H Bridge" (CHB). The isolation between the converters is achieved by the power supply. Interestingly, it was in the absence of PWM that multilevel conversion first developed. However, it was PWM that took over for the next decade, improving the waveform without adding any components [19].

It was not until the early 1980s that a new topology [20, 21] appeared, which combined an increase in the number of levels with PWM, thanks to more efficient active components, while offering advantageous sizing. In this topology, each component supports a fraction of the voltage thanks to an arrangement of diodes connected between each potential and the various active components. The first descriptions being proposed for 3 levels, the name adopted was "Neutral Point Clamped" or NPC, due to an intermediate potential connected to the neutral of the three-phase network [19].

The generalization of this structure requires adopting the name "Clamped Diode". This topology has become widely used in medium voltage variable speed drives and today remains the most widespread of the multilevel topologies [19]. Shortly afterwards, a reflection was undertaken on the value of the voltage levels naturally reducing the harmonics by using the topology of the digital-to-analog converter (DAC) [22]. This topology has an obvious simplicity, each level being connected to the common point of the filter, but imposes a heterogeneous dimensioning of the components. A. Nabae et al find this topology by proposing a variant of the NPC converter [20]. This structure consisting of a stack of switching cells on the different voltage sources, the name "Stacked Cell" (SC)

will be used here. These last two topologies have in common a DC bus divided by (N-1), (for a number of levels N), where each potential must obviously be controlled, which can be considered conditionally (depending on the operating point) by certain control strategies, or by a balancing structure. In any case, the increased complexity and cost limit the number of levels [19].

Also, the major interest of the series multicellular converter (1992, [23]) is to use floating voltage sources of decreasing amplitudes (which earned it its poetic name of "Flying Capacitors" (FC)) starting from an unfractionated DC bus, and with enough redundant states to ensure a natural balancing of the floating voltages, while evenly distributing the voltage across the terminals of each active component [19].

From the end of the 90s, the important diffusion that multilevel structures began to experience generated a large number of works which combined and improved these structures. Thus, combining the SC and FC topologies, the stacked multicell converter (also known as "Stacked Multicell Converter", SMC) makes it possible to reduce the energy stored in floating capacitors [24]. [25] offers a converter resembling the CHB, which does not require external power supplies for each module, called "Modular Multilevel Converter" (MMC), but whose operating conditions remain limited. A very fine analysis of the different possible sizing of the CHB converter was carried out by [26] and [27], independently varying the voltage of each H-bridge, which makes it possible to maximize the number of levels available, and to use for the PWM (at high frequency therefore) the low voltage cell with the best switching characteristics. Under certain conditions, the nourishment of the cells can be omitted, which improves the performance of these types of structures and could make them competitive.

Derived from nested cell (SC) and clamped diode (DC) converters with 3 voltage levels, the "Active NPC" [28] and "Stacked NPC" [29] converters have exactly the same characteristics (same types and same number). components carrying current for each level, same switching cells), and will therefore have the same efficiency as FC or NPC topologies. However, and this is their advantage, the redundancy of the switching cells, associated with an appropriate control, makes it possible to better distribute the losses among the active components and therefore to reduce the cooling system (or even to increase the specific power), however, at the cost of additional active components, but without floating capacitors. Considering that the losses due to the cooling system are secondary (but above all at a much lower cost compared to IGBTs), these topologies do not

differ from FC in terms of efficiency [19]. Fig. 1.14 illustrates some topologies of multilevel converters encountered in the literature [30].

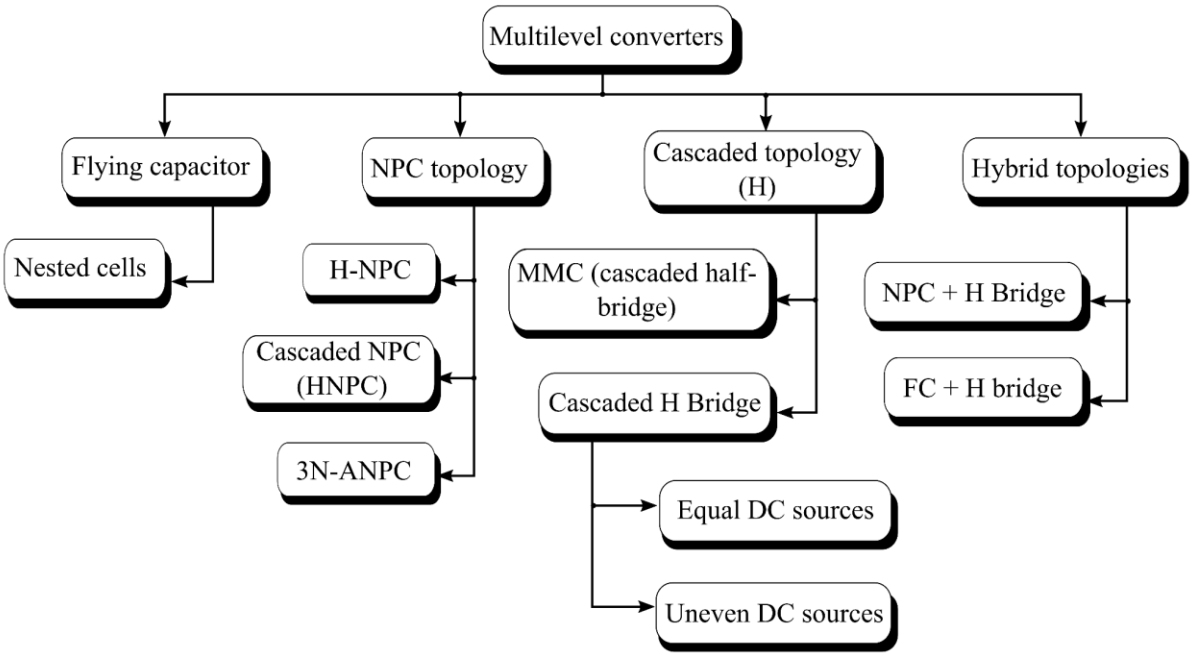


Figure 1.14 Classification of multilevel converters. [S.y]

The waveforms of multi-level inverters are shown in Fig. 1.15. We can see that the more the number of levels increases, the better the waveform (close to a sine wave).

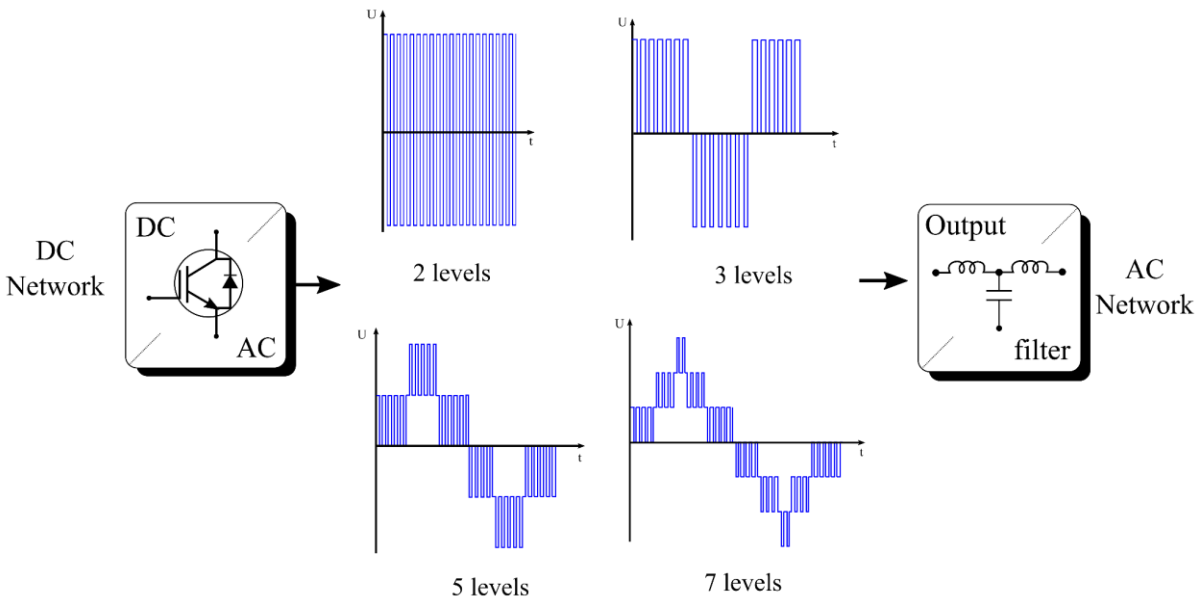


Figure 1.15 Principle of a multi-level inverter. [S.y]

We start by presenting the "series" multi-level inverters and subsequently those called "parallel" multi-level inverters will also be presented.

3.2.2.2.1 Multi-level series inverters

On the basis of the theory that several elementary cells are combined, series multi-level converters provide high voltage supply to medium and high power electric actuators, by splitting the input voltage at the converter (inverter or chopper). In addition, these techniques offer the advantage of obtaining higher quality current and voltage waveforms. This results in a reduction in current and voltage ripples and consequently in a reduction in losses due to high frequency harmonics.

These structures offer several advantages that can meet the different objectives of power injection into the electricity grid:

- They are intended for high voltage applications (railways, medium voltage electrical distribution networks with voltages of a few kilovolts)
- If the number of cells q is increased, The output voltage (and current) ripple amplitude of the converter decreases (see Eq. 1.7). This reduction in ripple leads to a reduction in the iron section of the magnetic circuits of the output filters, and therefore in the mass of the filtering.
- An increase in the apparent frequency of the current ripple and the output voltage (generally in $q.f_{sw}$), which also makes it possible to reduce the volume and / or the mass of the output filter [31].

There are different topologies of series multilevel inverters. We can cite among others:

- The topology of multi-level converters clamped by diodes: NPC (neutral point clamped). They are also called "distributed potential inverters"
- Inverters with cascaded converters in H-bridge.
- Nested cell inverters which are also called flying Capacitor inverters.

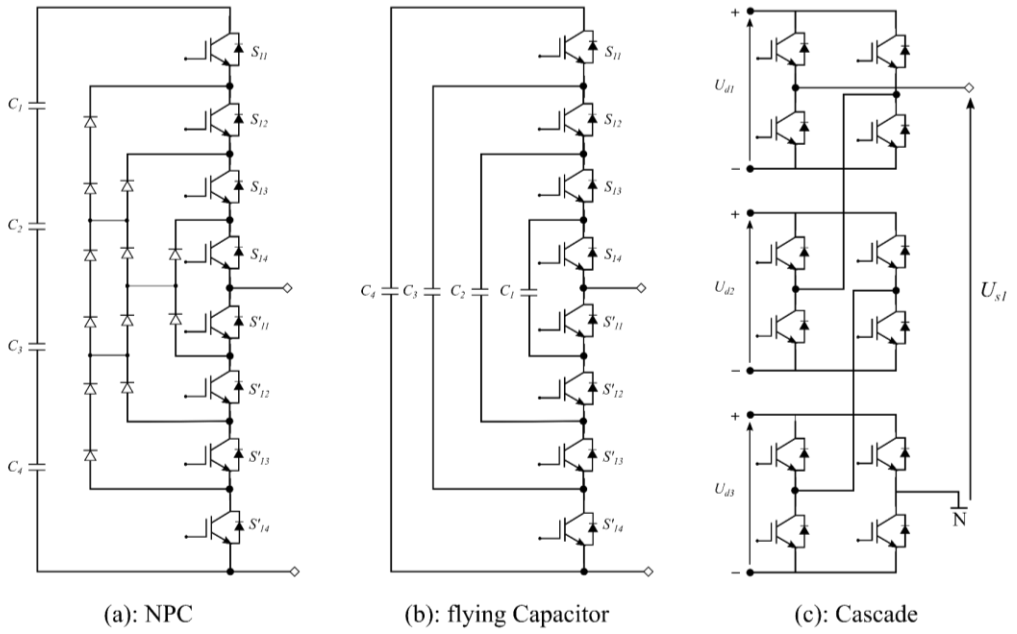


Figure 1.16 Series multilevel inverter topologies. [S.y]

a. NPC multi-level inverters

One of the reference structures in multilevel conversion is the 3-level NPC converter (Neutral Point Clamped). The objective of this multilevel inverter structure was to reduce the amplitude of the harmonics injected by the inverter into the load for motor power supply type applications [20], [21]. This structure, known as the neutral clamped converter, does not use an isolation transformer and the distribution of the voltage of the DC input on the various switches in series is ensured by the diodes (clamps) connected to capacitive midpoints.

Fig. 1.17 shows the electrical circuit corresponding to a 3-level inverter arm.

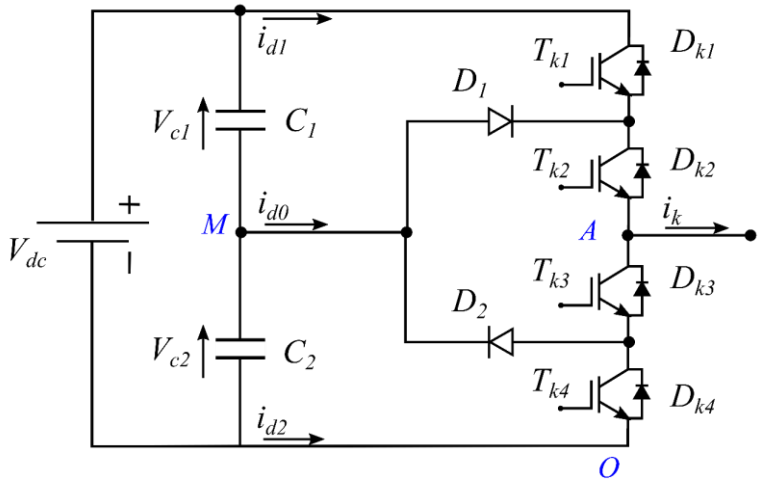


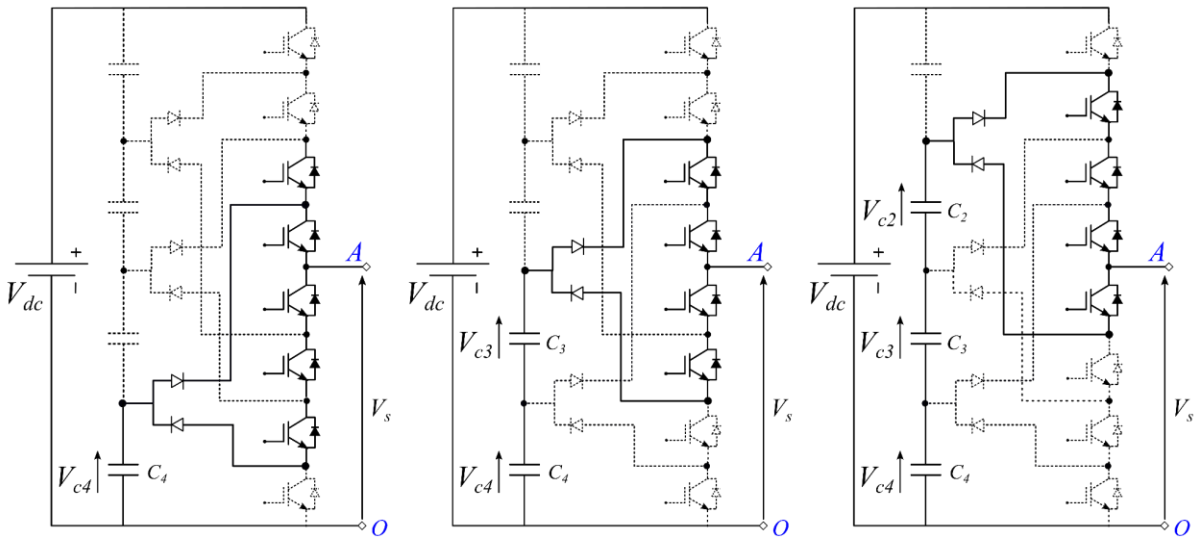
Figure 1.17 Arm of an inverter with NPC structure. [S.y]

This assembly is supplied by the direct voltage V_{dc}. The 3 possible switching states make it possible to deliver 3 distinct levels amid terminals A and M. Each branch has 2 stages each made up of 2 IGBT type switches with antiparallel diodes. The intermediate stages can be connected to midpoint M through two additional diodes D_1 and D_2. Table1.1 illustrates the method for producing the various voltage levels.

Table 1.1 Realization of the different levels for the NPC 3N inverter. [S.y]

Output voltage	Switches turned on	Direction of current	Current lows through ...
$V_{dc}/2$	T_{11}& T_{12}	$I_k > 0$	T_{11}& T_{12}
		$I_k < 0$	D_{11}& D_{12}
0	T_{12}& T_{13}	$I_k > 0$	D_1& T_{12}
		$I_k < 0$	D_2& T_{13}
$-V_{dc}/2$	T_{13}& T_{14}	$I_k > 0$	D_{14}& D_{13}
		$I_k < 0$	T_{14}& T_{13}

Every branch of the converter is seen as a switch whose positions allow the potential of point A to be modified. As illustrated in Fig. 1.19(b), this point is connected each time to one of the voltages through the capacitors, which sometimes are put in series. A switching configuration is shown in Fig. 1.18(a). The switches in dashed lines are open.



(a): 5-level inverter (1st level)

(b): 5-level inverter (2nd level)

(c): 5-level inverter (3rd level)

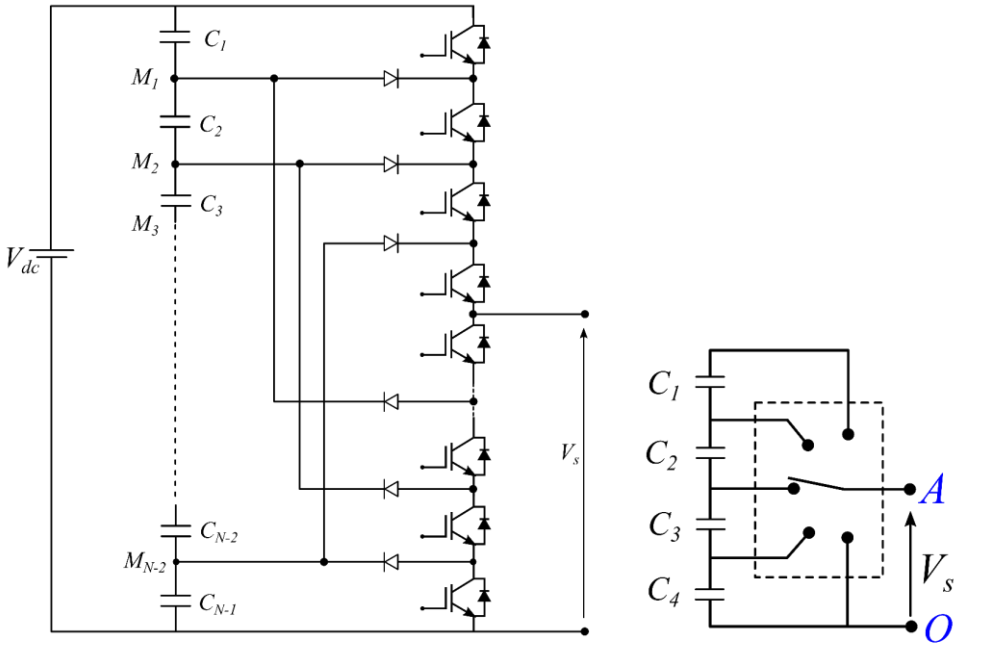
Figure 1.18 Principle of NPC topology. [S.y]

Fig. 1.18 shows the principle and the switching mechanism of a 5-level NPC inverter:

Fig. 1.18(a) represents the case where the inverter generates the 1st voltage level $V_s = V_{c4} = V_{dc}/4$.

Fig. 1.18(b) represents the case where the inverter generates the 2nd voltage level $V_s = V_{c4} + V_{c3} = 3V_{dc}/4$.

Fig. 1.18(c) represents the case where the inverter generates the 3rd voltage level $V_s = V_{c4} + V_{c3} + V_{c2} = 3V_{dc}/4$.



(a): Arm of an NPC inverter at N-levels (b): NPC fundamental principle

Figure 1.19 Generalization of the NPC structure. [S.y]

Fig. 1.19(b) illustrate the principle for which the action of power semiconductors is represented by an ideal switch with several positions. Each position represents a voltage level.

The structure of the NPC inverter was subsequently extended to increase the voltage and the amount of levels. The Fig. 1.19(a) shows the diagram of an NPC inverter arm at N voltage levels. Capacitors C_1 through C_{N-1} allow the input voltage to be split into N-1 fractions.

To obtain a voltage of N levels, N-1 capacities are necessary. The voltages at the terminals of the capacitors are all equal to V_{dc} / (N-1), V_{dc} is the complete voltage of the DC bus.

A set of N-1 capacitors makes it possible to create a set of N-2 capacitive midpoints having voltage potentials ranging from V_{dc} / (N-1), $2V_{dc}$ / (N-1), ... up to (N-2) V_{dc} / (N-1). Therefore, by connecting each of these points to the output and act on the control signal of the power switches, the arm output voltage is generated with an intermediate voltage.

Regarding the counting of the number of components, assets and liabilities, a three-phase NPC inverter with N-levels comprises:

- N-1 capacitors for the creation of capacitive midpoints. Each capacitor must be dimensioned for a voltage equal to V_{dc} / (N-1) and for a current equal to the maximum current of the load.
- 6 (N-1) fully controllable semiconductor type power switches plus an antiparallel diode for each.
- 6 (N − 2) clamp diodes.

The main advantages and drawbacks of NPC multilevel converters are as follows:

Advantages

- The resulting three-level waveform has better spectral quality compared to that of a conventional three-phase inverter, making passive filters less bulky.
- The DC bus for a 3-phase converter is shared across all phases. For this reason, a buck-to-buck topology is not only possible but also practical for uses such as a high voltage buck-to-buck interconnect or variable speed drive.

Drawbacks

- The voltage balance in the terminals of the capacitors becomes complicated, since it is closely linked with the power factor and the modulation index if the number of levels is larger than three.
- The inequality of the reverse voltages supported by the diodes.
- The inequality of switching between switches located outside the structure compared to others.

b. Nested cell multi-level inverters

Also called flying capacitor inverters, the structure is similar to that of the NPC inverter except that instead of using the clamp diodes, they are replaced by capacitors which act as the floating voltage sources from which it comes the name floating capacity inverter [32]. Nested cell inverters Fig. 1.16(b) have completely independent cells and offer the particularity of playing on an additional degree of freedom, in particular phase shift. This allows certain control strategies to use this phase shift to slightly offset the controls of the two cells and thus avoid the summation of the switching time gradients (dv/dt). It is also a means of balancing the voltages across capacitors.

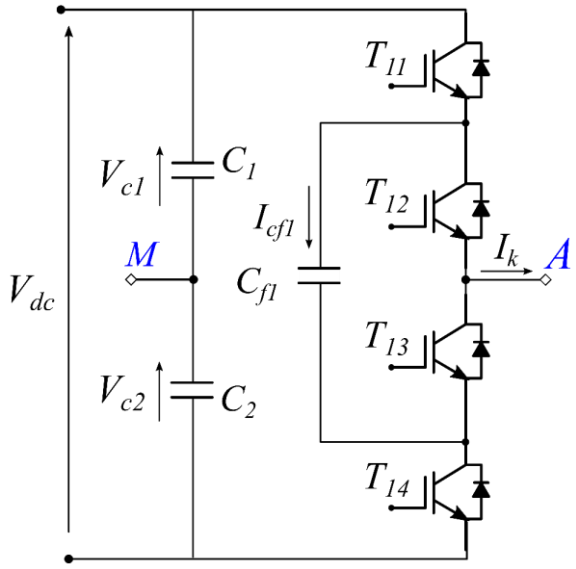


Figure 1.20 Three-level nested cell multilevel inverter arm. [S.y]

In its simplest version, the floating capacitor multilevel inverter is composed of four bidirectional switches & a capacitor placed between the intermediate stages for each arm, as well as two other capacitors allowing the DC bus to be split into two equal parts (Fig. 1.20).

Switches T_{11} and T_{12} are in the on state to have the positive voltage level $V_{dc}/2$, To have the negative voltage level -$V_{dc}/2$, it is the T_{13} and T_{14} switches which are in the on state, and to have voltage level 0, one of the following pairs of switches (T_{11}, T_{13}) or (T_{12}, T_{14}) must be on.

This redundancy is used to balance the flying capacitor C_{f1}, as the flowing output current in point A produces the negative flow (discharge) of the flying condenser, while the second produces positive current (charge), following the indications shown in Table 1.2.

Table 1.2 The voltage levels of the three-level flying capacitor inverter, the respective states of the switches and the currents of the flying capacities. [S.y]

Voltage level	State of switches				I_{cf} current
	T_{11}	T_{12}	T_{13}	T_{14}	
$V_{dc}/2$	1	1	0	0	0
0	1	0	0	1	$-i_k$
0	0	1	1	0	i_k
$-V_{dc}/2$	0	0	1	1	0

The Fig. 1.21 illustrates the block diagram of an inverter arm with p nested cells. Each pair of switches located on the same vertical forms a switching cell whose switches are controlled in a complementary manner. All combinations of control signals respecting this complementarity are authorized. Consequently, this inverter has 2 p potential control states. When the voltages at the capacitor terminals are equivalent, in its normal action the voltage at the capacitor terminals C_1 is equal to:

$$V_k = \frac{1}{p} . V_{dc} \qquad \text{(Eq.1.9)}$$

The voltage blocked by each power switch is given by the Eq. 1.10.

$$V_{blocking} = V_l - V_{l-1} = \frac{V_{dc}}{p} = \Delta V \qquad \text{(Eq.1.10)}$$

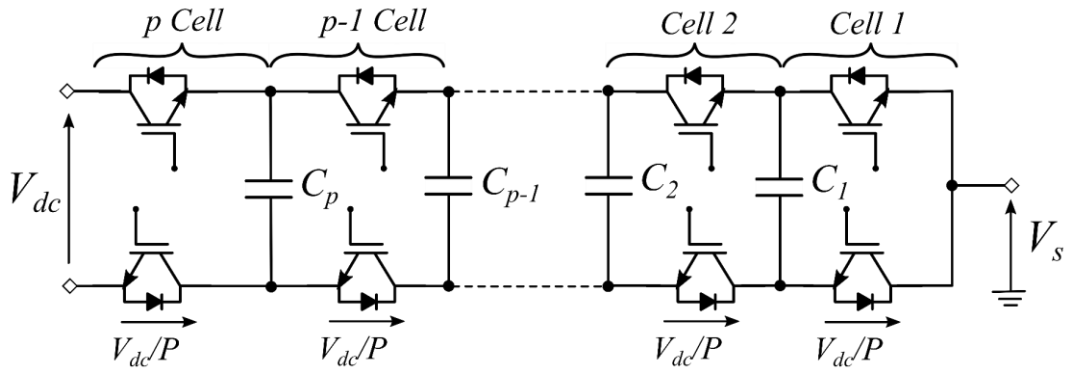


Figure 1.21 Schematic of the N-level nested cell multilevel inverter. [S.y]

This inverter is capable of generating $p+1$ distinct levels. It therefore has $2^p - p - 1$ switching states leading to redundant levels. To simplify the explanation, we will say that a switching cell is in the low state when the bottom switch is on, and that it is in the high state otherwise. A single combination leads to level 0: all cells are low. The p possible combinations for which a single switching cell is high lead to the V_{dc}/p level. The C_2^p combinations for which two switching cells are high lead to the $2V_{dc}/p$ level. So on, up to the V_{dc} level which can only be obtained when all cells are high [33].

The main advantages and disadvantages of nested cell multilevel converters are as follows:

Advantages

- The blocking voltage of the switches is the same everywhere.
- Its modularity allows easy extension and adaptation of control strategies to a high number of levels.
- Availability of redundant states balances capacitor voltage levels [34].

Drawbacks

- The main downside of this topology lies in the required number of capacitors, which can represent a prohibitive volume.
- The complexity to track the voltage levels for all capacitors.
- System control becomes difficult with increasing number of levels.

c. Cascaded inverters

Cascaded converter structures Fig. 1.16(c) are based on placing single-phase inverters in series in H-bridge. Indeed, the cascading of several 3-level structures (Fig. 1.22) makes it possible to have a multilevel voltage waveform at the output.

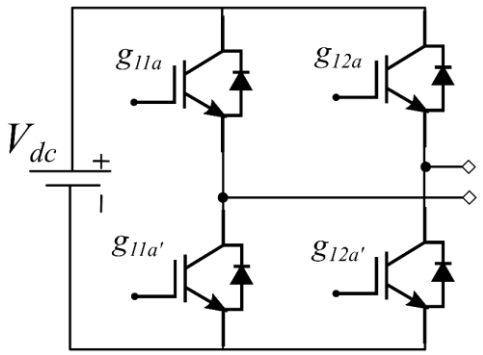


Figure 1.22 Full H-bridge. [S.y]

An independent isolated source is given for each H-bridge. In addition to ensuring natural voltage balancing, this topology enables a medium or high voltage load to be supplied from several low voltage sources. It is necessary to have as many sources as cascaded H bridges.

Fig. 1.23 shows the structure of a multi-level converter with N levels based on the series connection of single-phase inverters. The cells are connected there in a star [35]. Each partial cell is supplied by a direct voltage source. If the galvanically separated DC sources have the same level of direct voltage (V_{dc}), the phase voltage will be able to scale from level $(-H.V_{dc})$ to level $(+H.V_{dc})$ which will have N levels. Where $H = (N-1)/2$ is the number of all H-bridges or the number of separate DC sources [36]. As the number of voltage sources (V_{dc}) increases, there would be more levels in the output voltage. So the output voltage waveform will be closer to the sine wave [36].

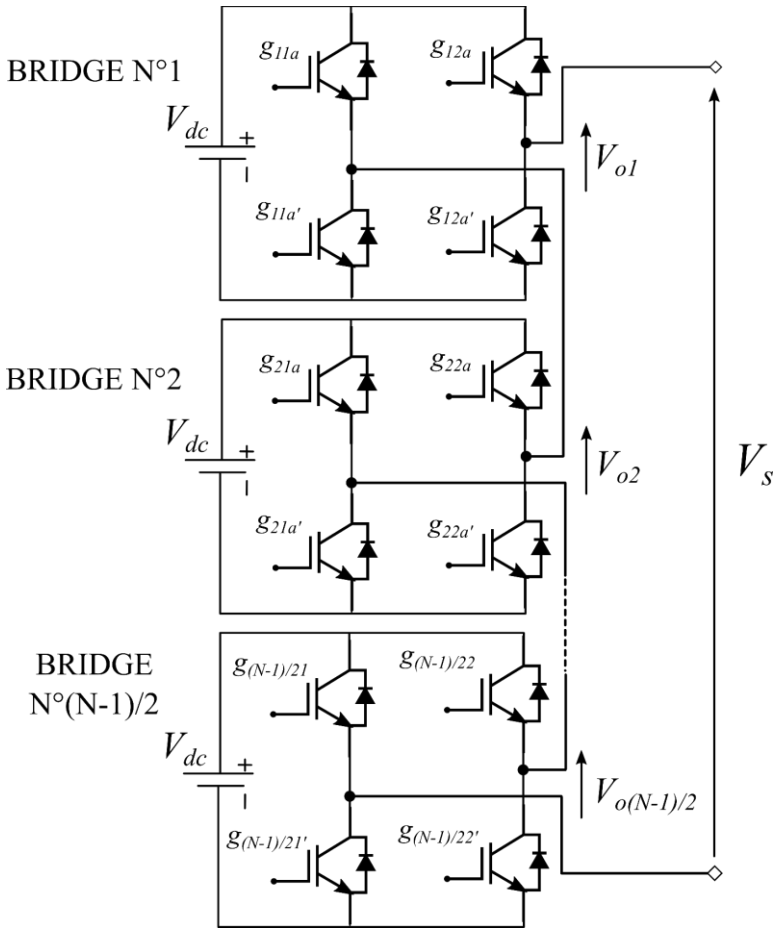


Figure 1.23 Structure of a multilevel inverter in H-bridges cascaded with N levels. [S.y]

The main advantages and disadvantages of nested cell multilevel converters are as follows:

Advantages [25]

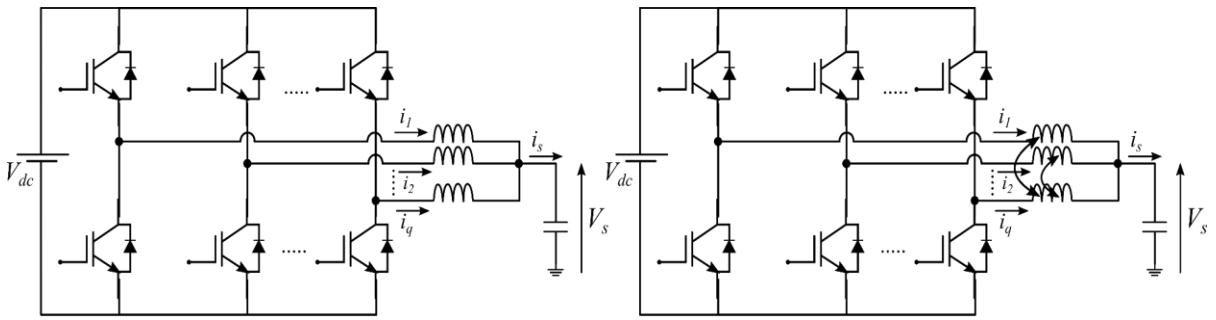
- The modularity of its structure easily allows its extension to a high number of cells in each phase, without additional complexity.
- The natural balancing of the voltages is achieved, so that the control of the switches is easily deviated.
- It becomes possible to supply a load with high or medium voltage from one or more low voltage supplies (for example in the case of photovoltaic energy).

Drawbacks

- It requires isolated DC voltage sources for each H bridge, which limits the application possibilities [34].
- It requires more power switches than a conventional inverter (and consequently the cost increase).

3.2.2.2.2 Parallel multi-level inverters

Parallel multi-level (multi-cell) inverters are mainly found in two forms: the interleaved inverter with independent inductors and the interlaced inverter with coupled inductors. These topologies lower the output filter volume by increasing the apparent frequency of the current ripple and the output voltage. Parallel placement of several cells can also accelerate the response time and increase the power density of the converter. Fig. 1.24 shows the two parallel inverter topologies.



(a): Interlaced q-cell inverter with independent inductors

(b): Interlaced q-cell inverter with coupled inductors

Figure 1.24 Parallel inverter topologies. [S.y]

a. Interlaced inverter with independent inductors

The interlace inverter with independent inductors provides attenuation of output current ripples. Indeed, the ripples of the output current are at the apparent frequency of the output current which is equal to q times the switching frequency [34]. With q is the number of cells. These ripples are expressed, in chopper operation, by the equation Eq. 1.11. In DC / AC operation, it is difficult to express these ripples because the duty cycle changes over time and the output voltage is also a function of time and depends on that of the network (in our case).

$$\Delta I_S = \frac{V_{dc}.\alpha'(1-\alpha')}{q^2.L.f_{sw}} \qquad \text{(Eq.1.11)}$$

With: ΔI_S is the output current ripple, V_{dc} is the DC voltage, α' is the output current's duty cycle. ($\alpha' = q\ .\ \alpha$, with α the control's duty cycle), q is the number of cells, L is the interleaving inductance and f_{sw} is the switching frequency.

However, converters based on this strategy allow an attenuation of current ripples only at the input and output of the system. The current ripples flowing through each inductor remain high and are at the switching frequency [34]. These ripples are determined (in DC / DC operation) as in the classical case, by the equation Eq. 1.12:

$$\Delta I_{cel} = \frac{V_{dc}.\alpha(1-\alpha)}{L.f_{sw}} \qquad \text{(Eq.1.12)}$$

It is evident from equation Eq. 1.8 that if the inductance L decreases, the ripples increase. The fall in the value of the filter inductances actually speed up the converter's response time, but increases the amplitudes of the current ripples in the cells. The losses in the semiconductors and in the windings of each cell increase due to the greater amplitude of the current ripples. There is therefore a compromise between efficiency and response time with this type of converter.

b. Coupled cell Interleaved Inverter

Coupling the inductors overcomes the drawbacks of the magnetically independent interlaced cell inverter. Indeed, a reduction in the ripples of the currents that pass through the inductors can be achieved by magnetically coupling the cells.

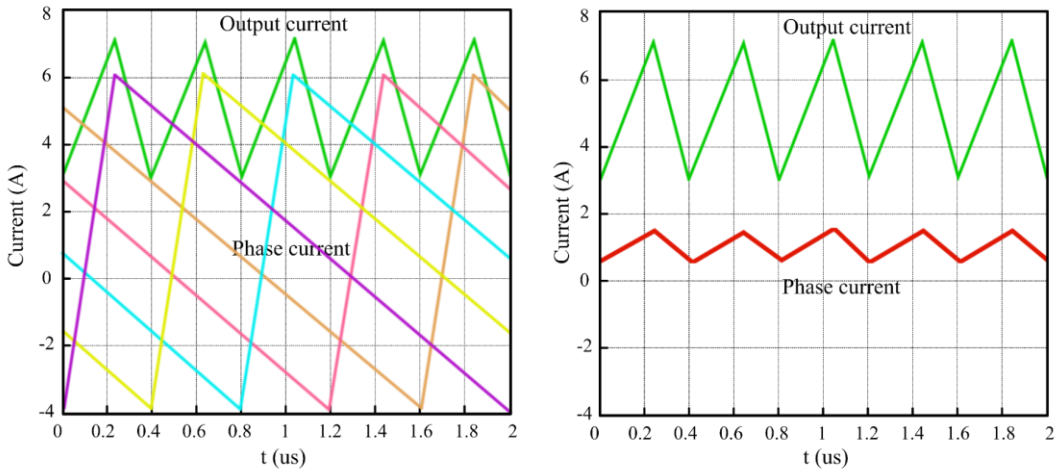


Figure 1.26 Effect of coupling of inductors on current ripples of cells. [S.y]

This Fig. 1.26, taken from the work of [31], shows a priori the interest of magnetic coupling between the different interlaced cells. The current ripple in the different cells is transposed to $q \times f_{sw}$ and reduced in amplitude. This makes it possible to choose inductances of low values and consequently to further reduce the volume of the output filter. System response time can also be reduced without sacrificing efficiency (low ripple).

The fact remains that coupling inductors also has drawbacks. For example, in the event of a differentiation between the various cells, with an interlaced inverter with magnetically coupled cells, one would risk losing control of the entire system. Since cells are magnetically coupled, an imbalance on one cell / phase would impact the other cells. This disqualifies this form of inverter for our use where the reliability and the charge of the system matter on the reduction of the volume (and the mass).

3.3 Passive filters for connection to the electrical grid

The role of passive filters for connection to the electrical network is to remove certain HF harmonics generated by the inverter in order to inject current into the electrical network in compliance with standards relating to network harmonics and electromagnetic compatibility. There are mainly two types of passive network connection filters: The L filter, and the LCL filter. Fig. 1.27 shows these passive filters.

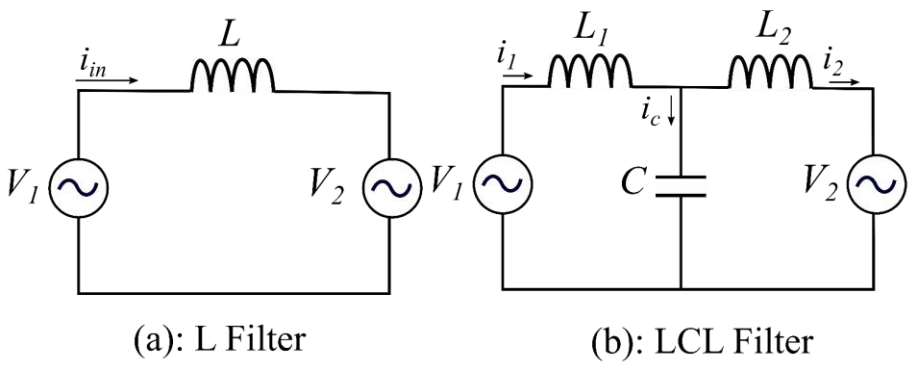


Figure 1.27 Passive filter topologies. [S.y]

V_1 and i_1 are the inverter output voltage and current, V_2 and i_2 are the network voltage and current, i_c is the current that passes through the capacitor, C is the filter capacitor L, L_1, L_2 are the inductances of the filter.

3.3.1 L filter

The basic filter used in the connection to the electrical network is composed of an inductor. This component is absolutely necessary to control the current between the two voltage sources that are the inverter and the network: it is therefore more than a filter but a functional element of the system, it also contributes to filtering harmonics in the first order of HF current. However, this simple filter does not allow sufficient attenuation of the harmonics of the current to be injected into the network. The L filter's transfer function, in the case where we neglect the internal resistance of the inductance and when V_2=0, is given to equation Eq. 1.13 (s is the Laplace operator).

$$H(s)_L = \frac{I(s)}{V_1(s)}\Big|_{V_2 = 0} = \frac{1}{L.s} \qquad \text{(Eq.1.13)}$$

To reduce the ripples, the value of the inductance should be increased, which slows down the current regulation dynamics and generates an increase in the volume and weight of the inverter. In addition, a significant voltage drop is produced with this filter at the mains frequency. The L-filter is more suitable for connecting a converter with a high switching frequency where the attenuation is sufficient [35].

3.3.2 LCL filter

The LCL filter is the structure most often used to connect an inverter to the grid [36]. It allows good attenuation of current harmonics even with low inductances. The LCL filter's transfer function when V2 = 0 is given in equation Eq. 1.14. The LCL filter achieves a better decoupling between the filter and the network impedance because it has an inductive output at the common point of connection to the network [35, 37, 38]. So, there are two main reasons for using an LCL filter at the expense of an L filter: first, for the same size (volume), the LCL filter has better attenuation than the L filter; secondly, The LCL filter prevents the voltage drop that could be caused by the L filter, and further reduces the ripple of the current to be injected into the grid.

$$H(s)_{LCL} = \frac{I_2(s)}{V_1(s)}\Big|_{V_2 = 0} = \frac{1}{L_1.C.L_2.S^3(L_1 + L_2)} \qquad \text{(Eq.1.14)}$$

4. Conclusion

This chapter has been devoted to the state of the art of photovoltaic systems connected to the electricity distribution network. We began this chapter by giving an overview of the general structures and the different architectures of the PV systems connected to the grid. In the second part, we approached a bibliographical study on the constituents of PV systems connected to the network. In particular, the basics of the solar cell and we reviewed the different topologies of static converters especially highlighting the multilevel concept and multilevel conversion history and showed the advantages and disadvantages of each element. Finally, we closed the chapter with an overview to passive filters to which our system will be connected to eliminate certain high frequency harmonics in order to compline with the standard relating to network harmonics compatibility and grid requirements.

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[S.y] Figures marked S.y are illustrated by Mr. Youcef Souda. Using varios softwares (inkscape, excel, photoshop…).

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Modeling of the constituents of the PV system conversion chain connected to the grid

Chapter outline

1. Introduction

Multi-level inverters allow high power to be conveyed without the components that constitute them undergoing considerable stress when they are controlled on opening as well as on closing. In order to generate a voltage source closest to the sinusoid, several control strategies have been proposed. Three conventional control strategies have always played a key function in the research work namely vector modulation, sinusoidal PWM and selective harmonic elimination.

This chapter deals with the detailed study of the NPC type three-level inverter (structure and principle of operation) and modeling of the inverter, then we will present the essential multilevel inverters control strategies, followed by digital simulations of the different strategies. In order to generalize the principles employed in the NPC topology.

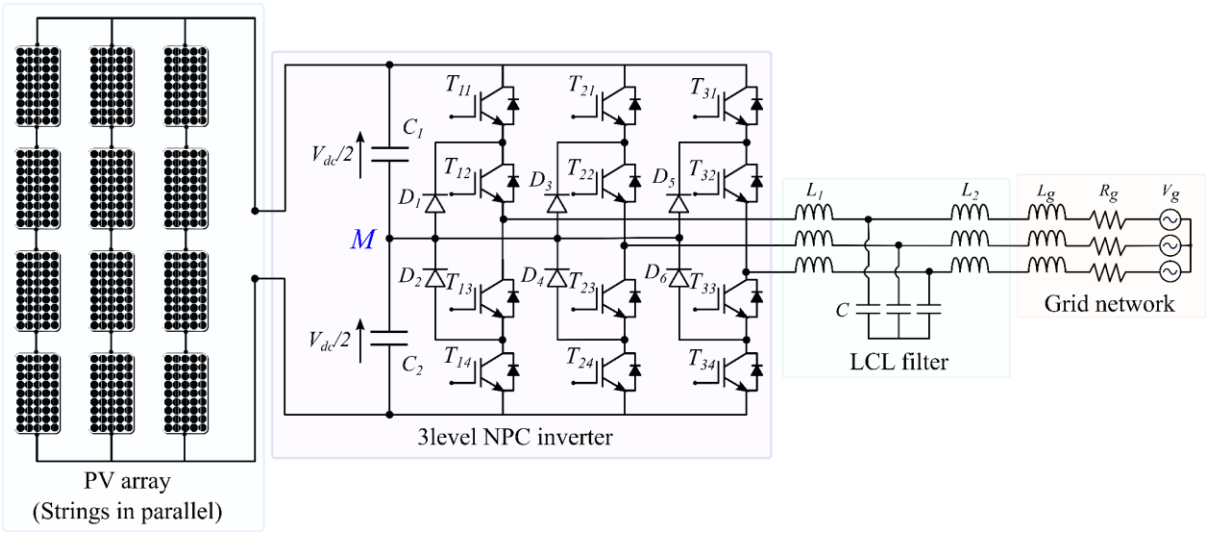

Figure 2.1 Diagram of the grid-connected PV system [S.y].

2. Modeling and modulation strategies of the NPC structure inverter

2.1 Three-level inverter structure

Fig. 2.2 shows the power circuit of the three-phase three-level inverter with NPC (Neutral Point Clamped) structure. Each arm of the inverter is made up of four pairs (Diode-Transistor) each representing a bidirectional switch and two middle diodes making it possible to have the zero level of the output voltage of the inverter. This structure requires the use of controllable switches for starting and blocking. In our case, we will use IGBTs with antiparallel diodes [1].

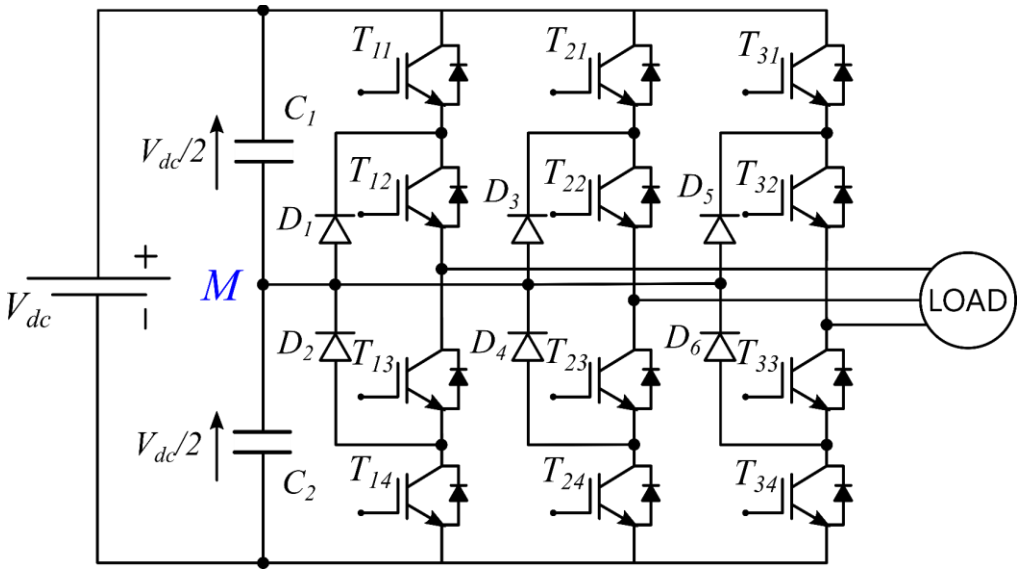

Figure 2.2 Three-level inverter with NPC structure [S.y].

2.2 Model of a bidirectional current switch

The switch can be defined as a dipole to establish an energy exchange between a source and a single-phase load. The synthesis switches to be implemented in an inverter must be bidirectional in current, with only one direction of flow of controllable loads. This function is performed by the association of a transistor, which is a switching switch controllable by external quantities, with an antiparallel diode, which is a spontaneous switch, depending only on internal quantities.

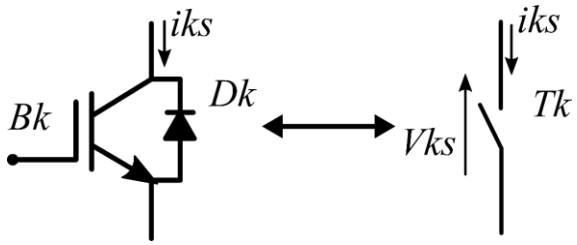

Figure 2.3 Bidirectional switch equivalent to the diode-transistor pair [S.y].

The transitions among its various configurations are only dependent on the external (control of semiconductor bases) control and thus on continuous conduction, a static converter is supposedly controllable, and consequently on continuous conduction. We will assume in the following that this condition is always verified. Under these conditions, we can define the concepts of connection function F_{ki} which translates the open or closed state of the switch T_{ki}. In order to have fully controllable operation that allows the inverter to deliver the three desired voltage levels, it must be operated in its controllable mode.

Three additional commands can be applied to an arm:

$$\begin{cases} B_{k1} = \overline{B_{k2}} \\ B_{k3} = \overline{B_{k4}} \end{cases} \quad \begin{cases} B_{k1} = \overline{B_{k3}} \\ B_{k2} = \overline{B_{k4}} \end{cases} \quad \begin{cases} B_{k1} = \overline{B_{k4}} \\ B_{k2} = \overline{B_{k3}} \end{cases} \qquad \text{(Eq.2.1)}$$

Of these commands, it is the second which gives the three voltage levels $V_{dc}/2$, 0 and -$V_{dc}/2$ in an optimal way.

Table 2.1 Excitation table associated with the complementary control.

B_{k1}	B_{k2}	B_{k3}	B_{k4}	V_{kM}
0	0	1	1	-$V_{dc}/2$
1	0	0	1	Unknown
0	1	1	0	0
1	1	0	0	$V_{dc}/2$

Table 2.1 shows the excitation table associated with this complementary command. (B_{ki}: Control of the base of the T_{ki} transistor)

2.3 Principle of operation

Fig. 2.4 illustrates the structure of the three levels inverter arm. The currents i_{d0}, i_{d1} and i_{d2} determine the direction of energy transfer of the conducting element (transistor-diode). The connection between the two sources is formed by the transistors when the voltage source is a generator, and the output current source

is a receiver. It is the diodes which guarantee the current flow when the transition from the outcome to the input source is made.

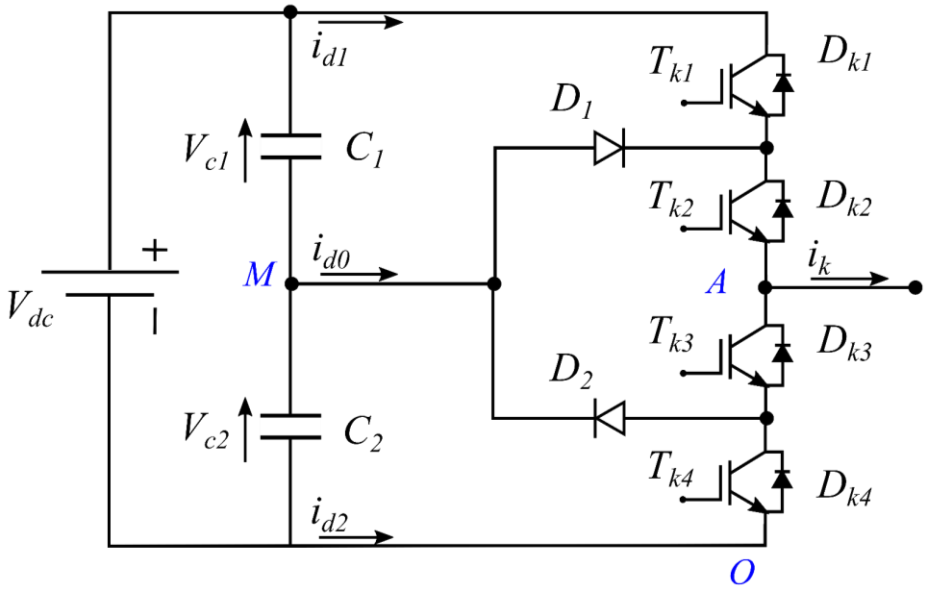

Figure 2.4 Three-level inverter arm [S.y].

A topological analysis of an arm shows three possible configurations for it. These different configurations are shown in Fig. 2.5.

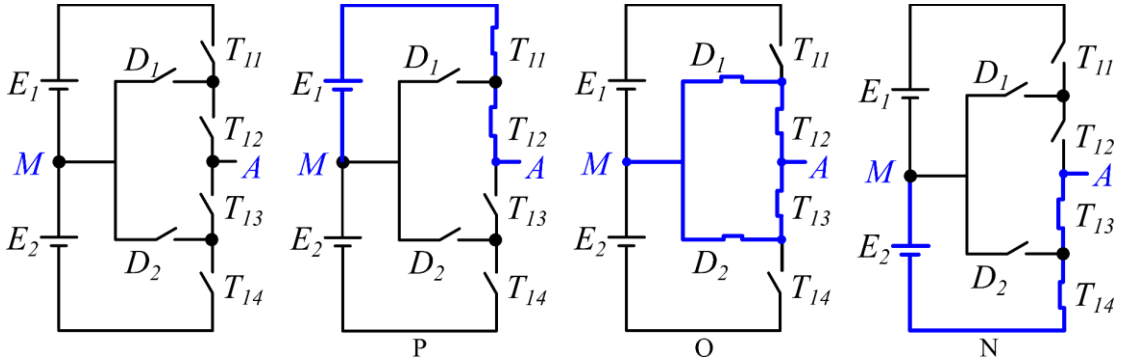

Figure 2.5 The different functional configurations of an arm [S.y].

2.4 States of an inverter arm

In controllable mode, each arm of the inverter has three possible states:

State P: The two T_{k1} and T_{k2} top switches (k = 1, 2, 3) are closed, while the two bottom switches T_{k3} and T_{k4} (k = 1, 2, 3) are open. The source neutral (M) output voltage is $V_{dc}/2$ respectively.

State O: The two middle switches T_{k2} and T_{k3} (k = 1, 2, 3) are closed, while the two end switches T_{k1} and T_{k4} (k = 1, 2, 3) are open. The source neutral (*M*) output voltage is 0 respectively.

State N: The two bottom switches T_{k3} and T_{k4} (k = 1, 2, 3) are closed, while the two top switches T_{k1} and T_{k2} (k = 1, 2, 3) are open. The source neutral (*M*) output voltage is -$V_{dc}/2$ respectively.

The correspondence between the states of the arm, the states of the switches and the output voltage is summarized in Table 2.2.

Table 2.2 States of an inverter arm (k = 1, 2 or 3)

Arm	Arm switch states				Output voltage
	T_{k1}	T_{k2}	T_{k3}	T_{k4}	
P	1	1	0	0	$V_{dc}/2$
O	0	1	1	0	0
N	0	0	1	1	-$V_{dc}/2$

2.5 Connection functions

Each switch k_{ij} assumed to be ideal introduces a connection function F_{ij} With:

$i = a, b, c$: indicator of the arm.

$j = 1, 2, 3, 4$: number of the switch of arm i.

This function is equal to 1 if the switch is closed, and 0 otherwise.

$$F_{ij} = \begin{cases} 1 \; if \; k_{ij} \; is \; closed \\ 0 \; if \; k_{ij} \; is \; open \end{cases} \quad \text{(Eq.2.2)}$$

The connection functions of the switches of the arm k are linked by the following relationships:

$$\begin{cases} F_{k1} = 1 - F_{k4} \\ F_{k2} = 1 - F_{k3} \end{cases} \quad \text{(Eq.2.3)}$$

With this additional control it all happens as if only two switching cells with two switches each are available for each arm of the inverter. These two cells are made

up of pairs of switches (T_{k1}, T_{k2}) and (T_{k3}, T_{k4}) respectively. A switching function F_{ki} associated with cell i of arm $k(i = 1\ or\ 2)$ is defined for the three-level inverter.

We call cell 1 of arm k the pair of switches (T_{k1}, T_{k2}) and cell 2 the pair (T_{k3}, T_{k4}).

Then we have: F_k^1: switching function associated with cell 1

F_k^2: switching function associated with cell 2

The switch connection functions are expressed using these switching functions as follows:

$$\begin{cases} F_{k1}(t) = \frac{1}{2}(1 + F_k^1(t)) \\ F_{k2}(t) = \frac{1}{2}(1 + F_k^2(t)) \end{cases} \quad \text{(Eq.2.4)}$$

$$\begin{cases} F_{k4}(t) = \frac{1}{2}\left(1 + F_k^1(t - \frac{T}{2})\right) \\ F_{k3}(t) = \frac{1}{2}\left(1 + F_k^2(t - \frac{T}{2})\right) \end{cases} \quad \text{(Eq.2.5)}$$

We define a connection function of the half-arm which we will denote by F_{kd}^b. With k: number of the arm, $d = 1$ for the upper half-arm and $d = 0$ for the lower half-arm.

For an arm that is expressed as follows in half-arm connection functions using the switch connection functions:

$$\begin{cases} F_{k1}^b = F_{k1} \times F_{k2} \\ F_{k0}^b = F_{k3} \times F_{k4} \end{cases} \quad \text{(Eq.2.6)}$$

F_{k1}^b is associated with the upper half-arm and F_{k0}^b is associated with the lower half-arm.

The connection functions of the three half-arms are:

$$\begin{cases} F_{11}^b = F_{11} \times F_{12} \\ F_{10}^b = F_{13} \times F_{14} \end{cases} \quad \begin{cases} F_{21}^b = F_{21} \times F_{22} \\ F_{20}^b = F_{23} \times F_{24} \end{cases} \quad \begin{cases} F_{31}^b = F_{31} \times F_{32} \\ F_{30}^b = F_{33} \times F_{34} \end{cases} \quad \text{(Eq.2.7)}$$

2.6 Multilevel inverter modulation strategies

For multi-level inverter control techniques, like SPWM, Selective Harmonics Elimination (SHE) and Vector Modulation, known as the Space Vector Modulation (SVM), the three key controls are considered [2]. The modulation methods employed in multi-level inverters can be categorized into two categories according to their switching frequencies: fundamental frequency and high frequency [3], shown in Fig. 2.6.

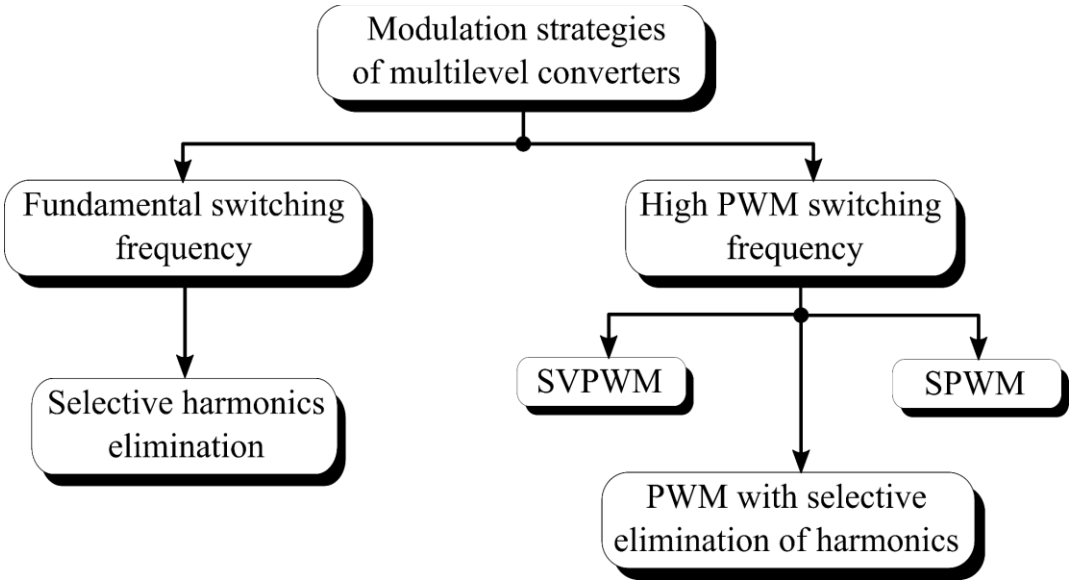

Figure 2.6 Multilevel inverter control strategies [S.y].

2.6.1 Fundamental frequency switching

2.6.1.1 Selective harmonics elimination

The idea for this strategy was first introduced by Turnbullen 1967, then developed by Patelet Hoften 1973 [4]. Its principle consists first of all in formulating the general expression of the amplitude of the harmonics, based on the development in Fourier series. The expression obtained is a function of the switching angles αi. Then, a system of nonlinear algebraic equations is obtained, imposing the desired value of the fundamental and canceling certain harmonics [5]. The resolution of this nonlinear system makes it possible to determine the switching angles αi, consequently the instants of control of the semiconductor switches.

Fourier series decomposition

Jean Baptiste Joseph Fourier presents the theory of the Fourier series. A sequence of periodic functions are the Fourier series. The aim is to disintegrate a periodic

signal into a set of sines and frequency cosines equal to the frequency of the base signal and in multiples. The following relationships will convey this mathematically:

$$S(t) = a_0 + \sum_{h=1}^{\infty} \{a_n \cos(h\omega t) + b_n \sin(h\omega t)\} \quad \text{(Eq.2.8)}$$

Where: $n \in N^*(1,2,3,\dots)$

The parameters a_0, a_n and b_n are said: Fourier coefficients. Their values give indications on the nature of the signal. We note that f_0 is defined as the base frequency (fundamental), and its multiples ($2f_0, 3f_0, \dots$) the harmonic frequencies.

The function $S(t)$ is therefore a continuous superposition of sinusoids whose frequencies take their values in the interval $[0,\infty]$.

$$\begin{cases} a_0 = \dfrac{1}{T}\displaystyle\int_{t_0}^{t_0+T} S(t)\,dt \\ a_n = \dfrac{2}{T}\displaystyle\int_{t_0}^{t_0+T} S(t)\cos(h\omega t)\,dt \\ b_n = \dfrac{2}{T}\displaystyle\int_{t_0}^{t_0+T} S(t)\sin(h\omega t)\,dt \end{cases} \quad \text{(Eq.2.9)}$$

With T: the period of the signal $S(t)$.

If the function $S(t)$ has real values, the Fourier coefficients are also reals. From Eq. 2.9, it is clear that the coefficient a_0 is nothing other than the average value of the signal $S(t)$ to be decomposed. This equation can be obtained by a simple integration of the expression of a_0 over a period T.

Symmetry with respect to the half-period

Functions with half-period symmetry have the following property:

$$S(t) = -S(t - \frac{T}{2}) \quad \text{(Eq.2.10)}$$

In this case, the development in Fourier series can be applied over a half-period $T / 2$ instead of T. The Fourier coefficients are as a result:

$$a_0 = 0 \quad \text{(Eq.2.11)}$$

$$\begin{cases} a_n = 0 & for\ n\ even \\ a_n = \frac{4}{T}\int_{t_0}^{t_0+T} S(t)\cos(h\omega t)dt & for\ odd\ n \end{cases} \quad \text{(Eq.2.12)}$$

$$\begin{cases} b_n = 0 & for\ n\ even \\ b_n = \frac{4}{T}\int_{t_0}^{t_0+T} S(t)\sin(h\omega t)dt & for\ odd\ n \end{cases} \quad \text{(Eq.2.13)}$$

Symmetry with respect to the quarter of the period

In this case the Fourier coefficients are as follows:

$$a_0 = 0 \quad \text{(Eq.2.14)}$$

$$a_n = 0 \quad \text{(Eq.2.15)}$$

$$\begin{cases} b_n = 0 & for\ n\ even \\ b_n = \frac{8}{T}\int_{t_0}^{T/4} S(t)\sin(h\omega t)dt & for\ odd\ n \end{cases} \quad \text{(Eq.2.16)}$$

From these relations we conclude that:

- the mean value is zero,
- the cosine terms are all zero,
- the even terms in sines are zero,
- only the odd terms in sines exist.

As a result, the Fourier series decomposition can be done over a quarter of the period.

Newton-Raphson method

In practice, the numerical analysis methods used to solve an implicit nonlinear algebraic equation of the following $f(x) = 0$, are based on Newton Raphson's method. This numerical analysis method iteratively determines the solution provided the derivative exists. Thus, starting from a solution $x^{(0)}$ quite close to the true solution x, we determine a better approximation by:

$$\begin{cases} x^{(1)} = x^{(0)} - \dfrac{f(x^{(0)})}{f'(x^{(0)})} \\ \vdots \\ x^{(n)} = x^{(n-1)} - \dfrac{f(x^{(n-1)})}{f'(x^{(n-1)})} \\ x^{(n+1)} = x^{(n)} - \dfrac{f(x^{(n)})}{f'(x^{(n)})} \end{cases} \quad \text{(Eq.2.17)}$$

Until the variance amongst the two consecutive values is negligible. This algorithm has a simple geometric interpretation since by writing the previous n^{th} equation in the following form:

$$f\left(x^{(n)}\right) = f'(x^{(n)})\left(x^{(n)} - x^{(n-1)}\right) \quad \text{(Eq.2.18)}$$

2.6.2 High frequency switching

2.6.1.1 Sinusoidal Pulse Width Modulation (SPWM)

The SPWM technique is among of the most common modulating techniques for multi-level inverters. In SPWM, a sinusoidal voltage wave called a reference is matched to a triangular wave called a carrier to generate the control signals for the switches of the inverter.

This strategy exploits the equivalence of the 3-level inverter to the 2-level inverters in series. Two identical carriers, phase-shifted from one another by half a chopping period ($1 / 2f_p$) can be used to improve the harmonics of the output voltages.

Different carriers are possible: triangular unipolar or bipolar carrier, unipolar or bipolar sawtooth carrier. The sawtooth carrier allows for the lowest harmonic rate but with even and odd harmonics. Triangular carriers allow output voltages to have quarter and half period symmetry.

the cases of two triangular unipolar and bipolar carriers are presented. That can be summarized in two steps:

Step 1: Determination of the intermediate voltages (V_{k0}, V_{k1})

$$\begin{cases} (V_{ref\,k} > U_{p1}) \Rightarrow V_{k1} = V_c \\ (V_{ref\,k} < U_{p1}) \Rightarrow V_{k1} = 0 \\ (V_{ref\,k} > U_{p2}) \Rightarrow V_{k0} = 0 \\ (V_{ref\,k} < U_{p2}) \Rightarrow V_{k0} = -V_c \end{cases} \quad \text{k=1, 2, 3} \quad \text{(Eq.2.19)}$$

Step 2: Determination of signal V_{k2} and switch control orders:

$$\begin{cases} V_{k2} = V_{k1} + V_{k0} \\ V_{k2} = U_c \Rightarrow T_{k1} = 1, T_{k2} = 1 \\ V_{k2} = -U_c \Rightarrow T_{k1} = 0, T_{k2} = 0 \\ V_{k2} = 0 \Rightarrow T_{k1} = 1, T_{k2} = 0 \end{cases} \quad \text{k=1, 2, 3} \quad \text{(Eq.2.20)}$$

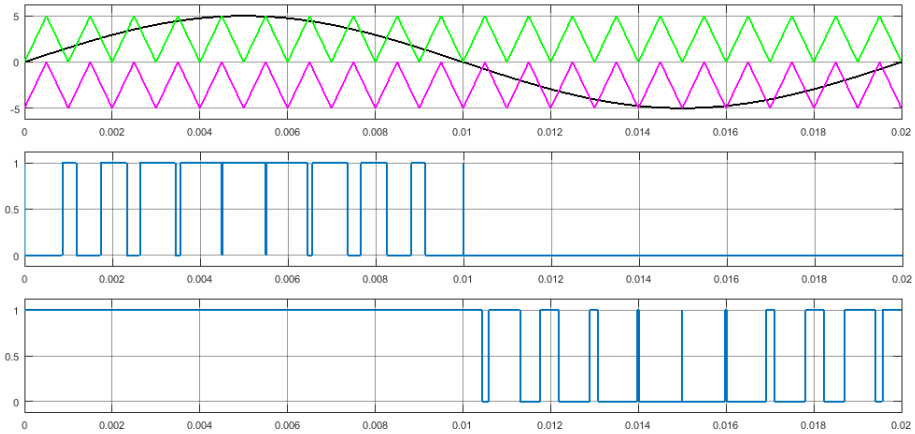

Figure 2.7 Principle of sinusoidal PWM with two unipolar carriers [S.y].

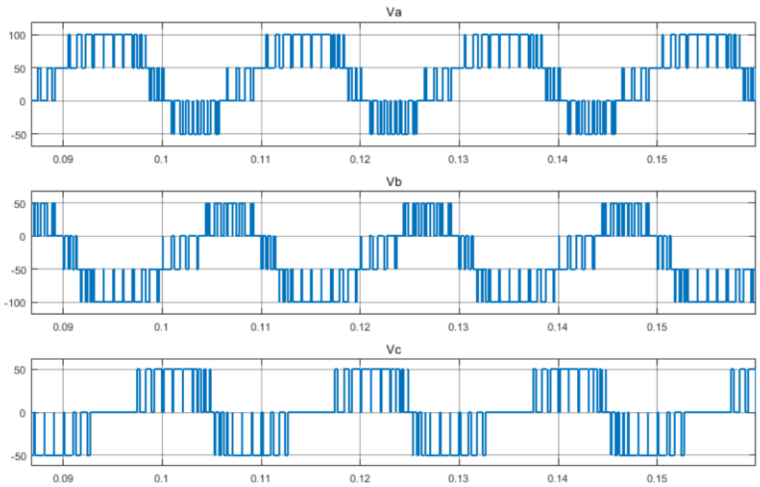

Figure 2.8 Voltage & charge current of the 1st phase [S.y].

2.6.1.2 Space vector PWM (SVPWM)

a. Principle of SVPWM

A multi-level inverter alternate control technique is known as the SVPWM (Vector PWM), which employs a command deviation from a control system and identifies each switching vector to a point in complex spaces. (d,q)

In terms of efficiency, the SVPWM technique is unanimous among researchers compared to that of PWM. This is because the maximum voltages supplied by an inverter controlled with the SVPWM technique are higher than that controlled with that of the PWM. We have:

$$V_{max_{(SPWM)}} = V_{dc}/2 \;\&\; V_{max_{(SVPWM)}} = V_{dc}/\sqrt{3} \qquad \text{(Eq.2.21)}$$

Which implies: $V_{max_{(SVPWM)}} > V_{max_{(SPWM)}}$

This means that with the SVPWM, we are able to have a voltage of 15% of V_{dc} more than the PWM. However, due to the large number of switching states, the SVPWM algorithm is more intricate than the PWM algorithm. This algorithm consists of six essential steps. At the level of each step, there are several calculation methods. The steps are as follows [6]:

Determination of the reference voltage vector

- Calculation of the sector.
- Calculation of the region.
- Calculation of switching times.
- Calculation of switching sequences.
- Generation of PWM signals.

3. Electrical design of the LCL filter

Mathematical models presented in this thesis are made based on the following considerations: 1) the parasitic resistances of inductors and capacitors of filter are discarded because the inductive and capacitive reactance are much larger than the parasitic resistances, 2) the utility grid is considered as an ideal voltage source, i.e. the grid has impedance equal to zero, and 3) the grid supplies power to fundamental frequency (50Hz).

Transfer functions that relate output current with input voltage are obtained based on the equivalent circuit for one phase of the three-phase system, facilitating mathematical analysis. LCL filters can be modeled by linear equations; i.e., filters meet principles of superposition and homogeneity. Transfer functions are obtained by Laplace transform.

3.1 Mathematical model of LCL filter

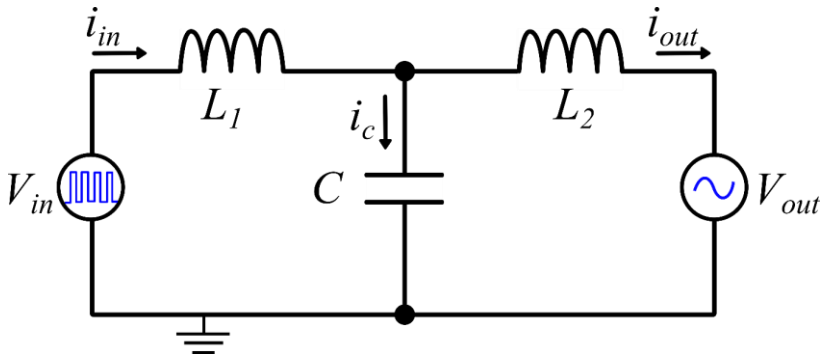

Figure 2.9 Schematic diagram of LCL line filter [S.y].

Mathematical deduction of LCL filter's model of Fig. 2.9 is shown in Eq. 2.22 to Eq. 2.26.

$$i_{in} = i_c + i_{out} \quad \text{(Eq.2.22)}$$

$$V_{in} = s.L_1.i_{in} + \frac{1}{s.c}.i_c \quad \text{(Eq.2.23)}$$

$$V_{out} = -s.L_2.i_{out} + \frac{1}{s.c}.i_c \quad \text{(Eq.2.24)}$$

Assuming that the filter is ideal, harmonics higher that the fundamental harmonic do not appear in the output current of LCL filter. The reason is that the V_{out} source can be regarded in the mathematical model as a short circuit, i.e.

$V_{out} = 0$. Thus, by replacing in Eq. 2.36 and solving for i_c it is obtained:

$$i_c = s^2.c.L_2.i_{out} \quad \text{(Eq.2.25)}$$

Substituting Eq. 2.22 & Eq. 2.25 in Eq. 2.23 and solving for i_{out}/V_{in} the transfer function that models the dynamic behavior of the LCL filter is obtained in Eq. 2.26.

$$\frac{i_{out}}{V_{in}} = \frac{1}{s^3.c.L_1.L_2 + s(L_1 + L_2)} \quad \text{(Eq.2.26)}$$

LCL filter's resonance frequency (f_0) is presented in Eq. 2.27.

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1.L_2.c}} \quad \text{(Eq.2.27)}$$

Capacitive reactance of the LCL filter is presented in Eq. 2.28.

$$X_c = \frac{1}{\omega.c} \quad \text{(Eq.2.28)}$$

3.2 Design criteria of LCL filter

Design of LCL filters requires inductors and capacitors to ensure the reduction of high frequency harmonics, to ensure reduction of THD and to meet the standards of quality energy. Design of LCL filters should consider the following functional [9, 10].

- Maintain low power losses in the filter, preventing voltage attenuation larger than desired.
- Avoid significantly influencing the bandwidth of LCL filter on the existing current control system bandwidth.
- Ensure that the size, weight and economic cost of the filter elements are low.

a. Design of L_1 Inductor

High values of L_1 and L_2 allow to reach very low levels in the current ripple. However, the inductors with high value have high weight, volume and cost. Reason why, the design values of L_1 and L_2 inductors should maintain a compromise between reducing the current ripple and size and cost of the inductor.

The value of the L_1 inductor can be approximated, assuming a voltage drop in L_1 is less than 5% of the nominal voltage of the grid, i.e.

$$V_{L_1} \leq 0.05\ .V_{line} \quad \text{(Eq.2.29)}$$

Where V_{L_1} is the voltage drop over L_1 and V_{line} is the effective voltage on the grid (RMS).

$$V_{L_1} = L_1.\frac{\Delta i_{out}}{\Delta t} = L_1.\frac{\Delta i_{out}}{\delta.T_{sw}} = L_1.\frac{\Delta i_{out}.f_{sw}}{\delta} \quad \text{(Eq.2.30)}$$

Where Δi_{out} is the maximum ripple that is expected in the current i_{out}, δ is the maximum width of the PWM modulation signal in the power inverter, f_{sw} is the switching frequency and T_{sw} is the switching period.

Equaling equations Eq. 2.29 & Eq. 2.30, expression for calculating minimum value of L_1 is obtained.

$$L_1 \leq \frac{0.05\ .V_{line}.\delta}{\Delta i_{out}.f_{sw}} \quad \text{(Eq.2.31)}$$

b. Design of L_2 Inductor

The range $5 < \frac{X_{L_1}}{X_{L_2}} < 10$ allows to reach low amplitude ripples in the output current, preserving low volume, low weight and low cost in the inductors [9]. The following equation allows to calculate approximate value of the inductor L_2.

$$\frac{1}{10}\ .L_1 \leq L_2 \leq \frac{1}{5}\ .L_1 \quad \text{(Eq.2.32)}$$

c. Design of C Capacitor

Capacitor value is selected to achieve increased attenuation near to switching frequency, producing a low reactance at the grid frequency. The capacitor must absorb little reactive power to the grid frequency, preventing a significant increase of current in the inductor L_1.

Reactive power in capacitor Q_C can be calculated by the following expression:

$$Q_C = 2\pi.f_{net}.C.{V_{line}}^2 \quad \text{(Eq.2.33)}$$

f_{net} is the utility grid frequency and C is the filter capacitance.

To maintain low Q_C in comparison with the nominal active power of power inverter (P), Q_C is selected such that

$$15\%\, P \leq Q_C \leq 25\%\, P \qquad \text{(Eq.2.34)}$$

Active power P can be calculated in a three-phase system by:

$$P = \sqrt{3}\,.V_{line}.I_{line}.\cos(\varphi) \qquad \text{(Eq.2.35)}$$

Where I_{line} is the nominal current of the line and $\cos(\varphi)$ is the power factor.

Selecting $Q_C = 20\%\, P$ and equating to Eq. 2.35, the following equation is obtained:

$$C = \frac{0.02\,.P}{Q_C} \qquad \text{(Eq.2.36)}$$

Capacitor impedance at switching frequency should be lower than impedance of the inductor L_2, allowing high frequency harmonics to be mitigated by the presence of the capacitor C Such that:

$$\frac{1}{10}\,.X_{L_2} \leq X_C \leq \frac{1}{5}\,.X_{L_2} \qquad \text{(Eq.2.37)}$$

The value of capacitor C should be selected such as to meet the expressions (2.36) and (2.37).

4. Conclusion

In the first half of this chapter a three-phase mathematical inverter model with NPC structure could be established. Then, we presented the major multi-level inverter control modulation strategy vector pulse width (SVPWM), selective harmonic elimination and sinusoidal PWM.

Furthermore, Inappropriate LCL-Filter design can result in high voltage attenuation at the inverter output, resonances and oscillations can increase THD, power system instability and slow dynamic response. The systematic LCL filter design can alleviate these inconveniences and simplify the LCL filter design. The LCL filter reduces ripple current and voltage at the inverter output, allowing to meet the quality standards of energy. The LCL filter also enables the inverter to be tied to the grid, thereby enhancing the power system performance.

In the next chapter we will proceed to further explain the control strategies chosen for our simulation system.

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Control strategies of the grid-connected PV system

Chapter outline

1. Introduction

In the case of grid connected PV system, dynamic control strategy is essential to harness the solar energy efficiently as well as for an energy optimization. This chapter is dedicated for the main control methods of the components of the system, we will start off by explaining the modulation strategy of the multi-level inverter for the generation of the control signals for the switches. In the second part of this chapter we will focus on the maximum power point tracking for the PV array.

At any moment the operating point of a PV array depends on insolation levels, temperature and the load of the system. The atmospheric conditions and load variables are changing constantly making it very difficult to extract all of the solar energy available from panels without a controlled system. With the use of maximum power point tracking algorithms along with power electronic converters maximum power is extracted from the array [1].

2. Sinusoidal pulse width modulation (SPWM)

The width of all pulses the same as in the case of multiple PWM, the width of each is varied in proportion to the amplitude of a sine wave evaluated at the same pulse [2]. The distortion is reduced significantly compared to multiple PWM [3]. A high frequency triangular wave, called the carrier wave, is compared to a sinusoidal signal representing the desired output, called the reference wave. Usually, ordinary signal generators produce these signals. Whenever the carrier wave is less than the reference, a comparator produces a high output signal, which turns the upper transistor in one leg of the inverter ON and the lower switch OFF. In the other case the comparator sets the firing signal low, which turns the lower switch ON and upper switch OFF [4]. The number of pulses per half cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm cannot conduct at the same time, the instantaneous output voltage is shown in Fig. 3.1 [5]. The output voltage can be varied by varying the modulation index "*m*".

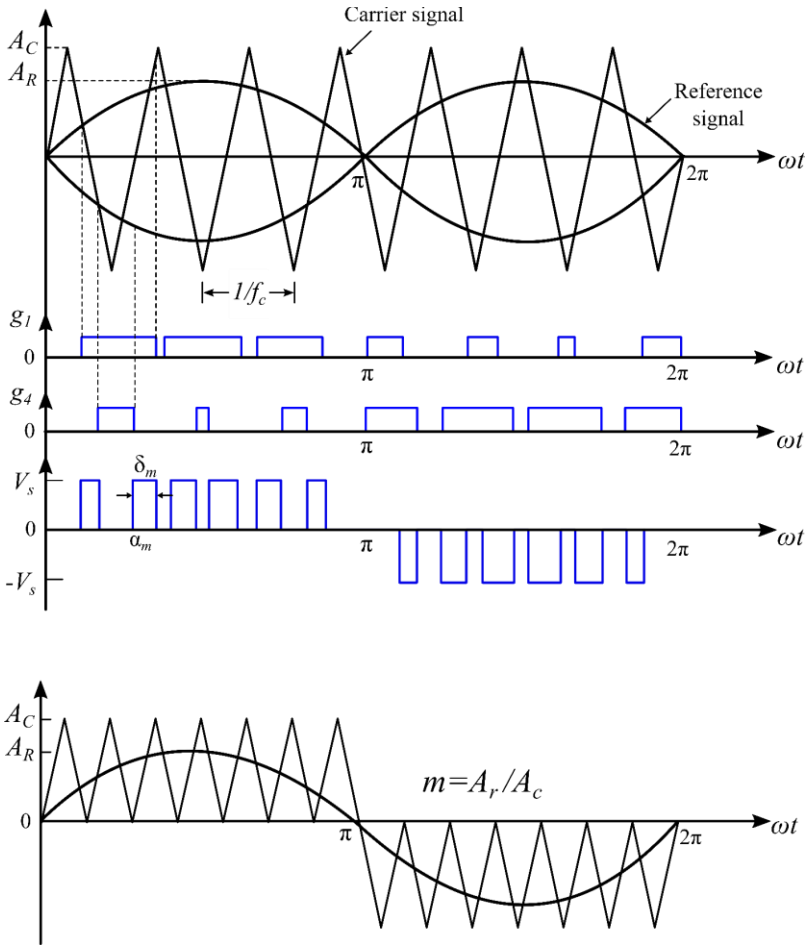

Figure 3.1 SPWM generating gate pulses [S.y].

The area of each pulse corresponds approximately to the area under the sine wave between the adjacent mid points of off-periods on the gating signals. The SPWM, which is most commonly used, suffers from certain draw back like low fundamental output voltage [4].

Alternative Phase Opposition Disposition (APOD), where carriers in adjacent band are phase shifted by 180° are shown in Fig. 3.2.

Phase Opposition Disposition (POD), where carriers above the reference zero point are out of phase with those below zero by 180° are depicted in Fig. 3.3.

Phase Disposition (PD), where all carriers are in phase across all bands is shown in Fig. 3.4.

Variable frequency carrier (VFC), where two carriers above and below the zero point have different frequency is shown in Fig. 3.5.

MATLAB/Simulink was used to implement the different SPWM techniques simulation of the inverter.

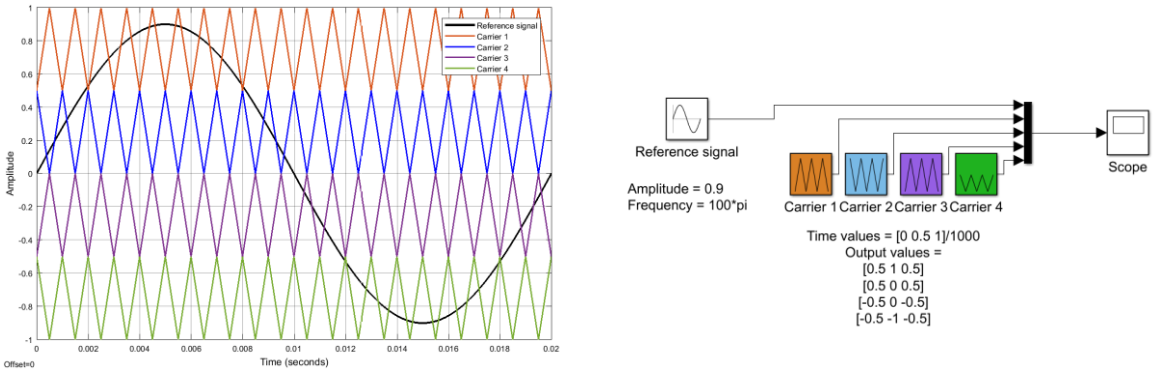

Figure 3.2 Alternative Phase Opposition Disposition (APOD) [S.y].

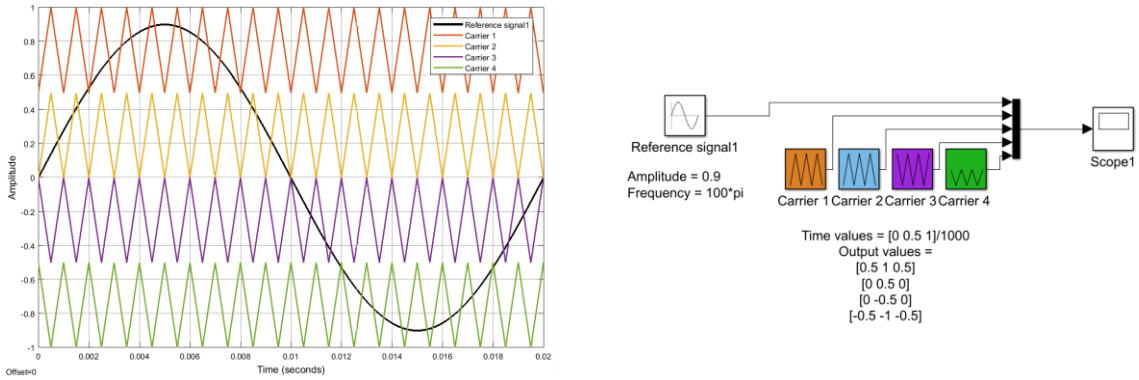

Figure 3.3 Phase Opposition Disposition (POD) [S.y].

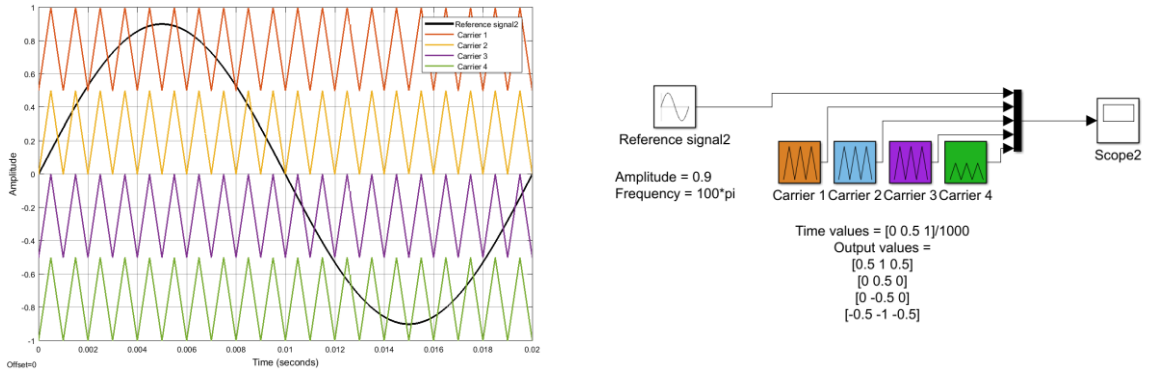

Figure 3.4 Phase Disposition (PD) [S.y].

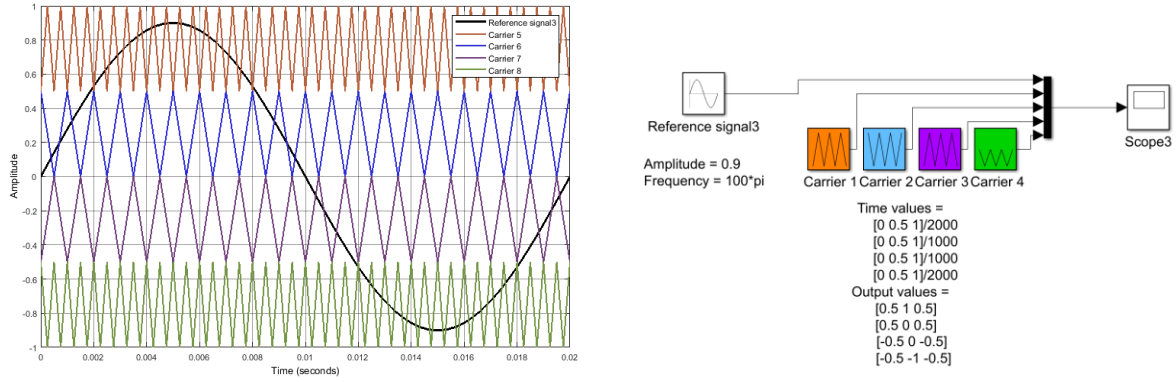

Figure 3.5 Variable frequency carrier (VFC) [S.y].

Application to the 5 level flying capacitor NPC inverter:

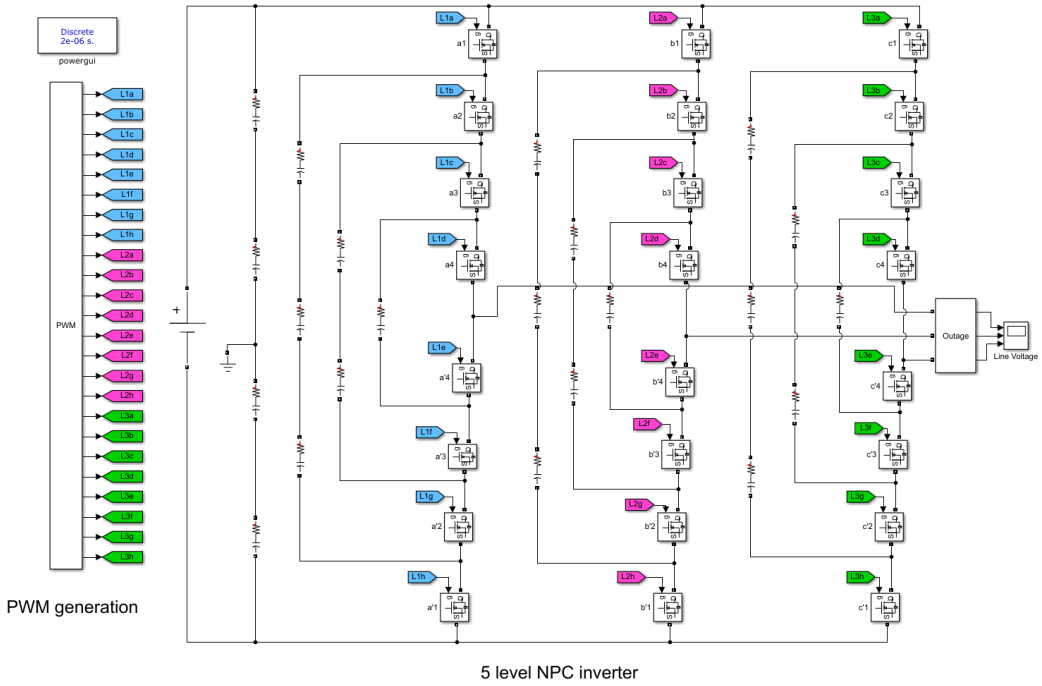

Figure 3.6 Simulation diagram of a 5 level NPC flying capacitor inverter using matlab simulink [S.y].

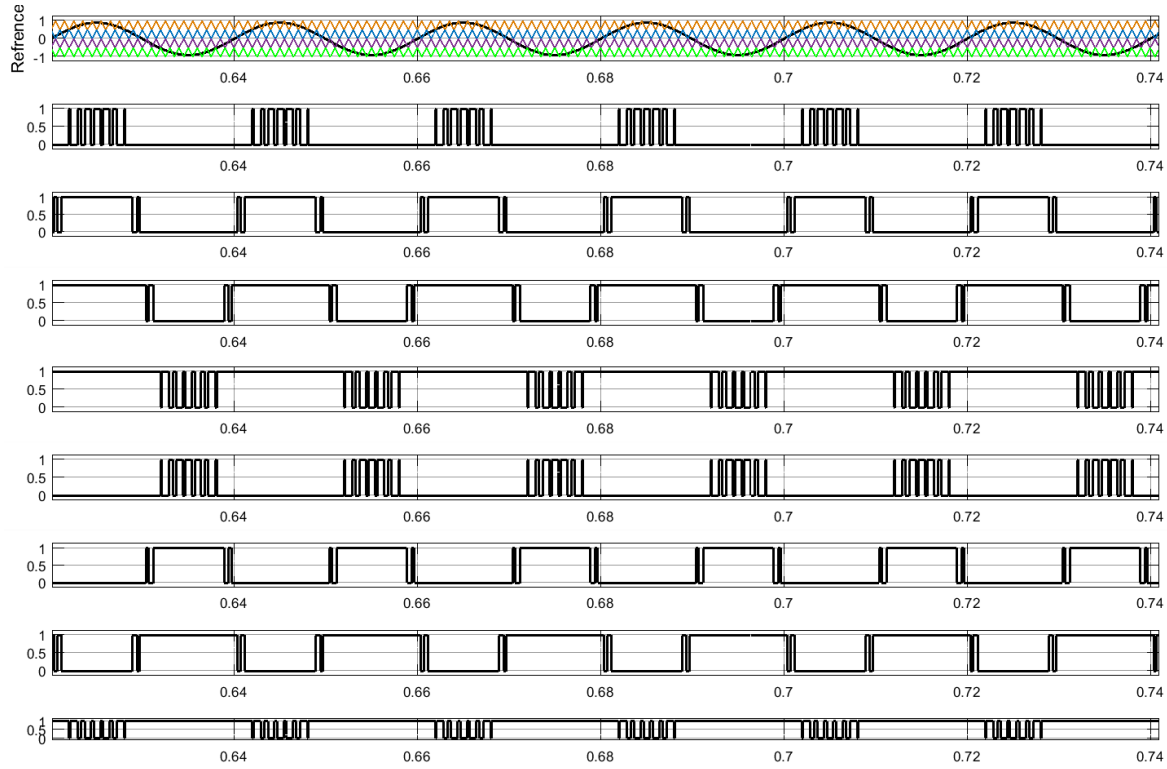

Figure 3.7 PWM generation employing Alternative Phase Opposition Disposition (APOD) [S.y].

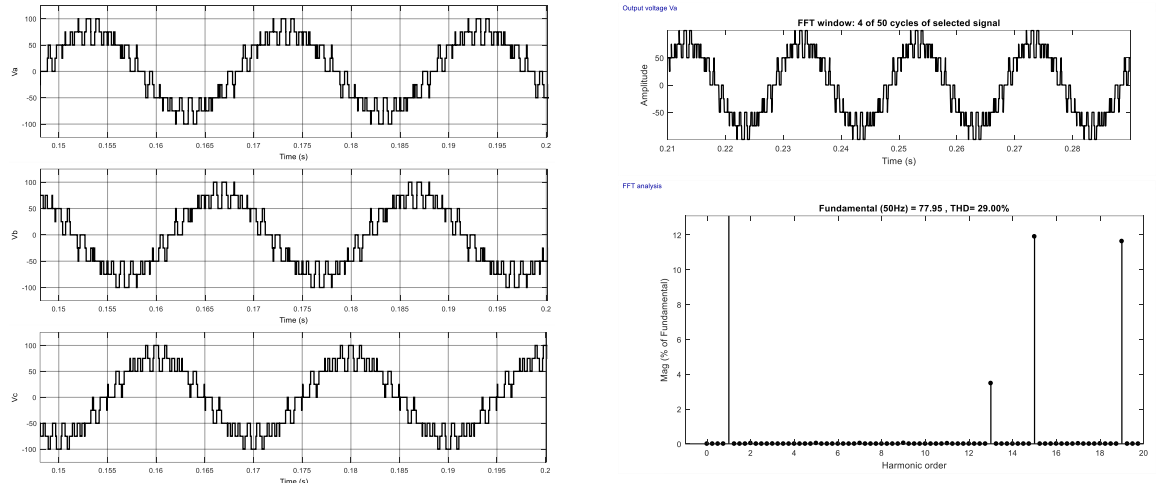

Figure 3.8 Output voltages with FFT analysis employing APOD modulation strategy [S.y].

Fig. 3.8 illustrates the output voltages of the flying capacitor NPC inverter employing Alternative Phase Opposition Disposition (APOD) as the modulating technique. As seen in Fig. 3.8 the phase voltage has a THD level of 29.00%

3. Incremental conductance MPPT method

The objective of maximum power point tracking is to adjust the actual operating voltage of an array according to the voltage corresponding to maximum power [6]. The basic idea of IC based MPPT is, at the maximum power operating point the derivative of the power with respect to the voltage is equal to zero [7]. From Fig. 3.11 note that to the left of the MPP the power is increasing with the voltage, i.e. $dP/dV > 0$, and it is decreasing to the right of the MPP [1], i.e. $dP/dV < 0$. This can be written in the following equations.

$$\frac{dP}{dV} = 0 \text{ at the MPP} \quad \text{(Eq.3.1)}$$

$$\frac{dP}{dV} > 0 \text{ to the left of the MPP} \quad \text{(Eq.3.2)}$$

$$\frac{dP}{dV} < 0 \text{ to the right of the MPP} \quad \text{(Eq.3.3)}$$

Writing these equations in terms of the array current and voltage using:

$$\frac{dP}{dV} = \frac{d(I.V)}{dV} = I + V.\frac{dI}{dV} \quad \text{(Eq.3.4)}$$

$$\frac{dI}{dV} = -\frac{I}{V}\left(\frac{dP}{dV} = 0\right) \text{ at the MPP} \quad \text{(Eq.3.5)}$$

$$\frac{dI}{dV} > -\frac{I}{V}\left(\frac{dP}{dV} > 0\right) \text{ at the left of MPP} \quad \text{(Eq.3.6)}$$

$$\frac{dI}{dV} < -\frac{I}{V}\left(\frac{dP}{dV} < 0\right) \text{ at the right of MPP} \quad \text{(Eq.3.7)}$$

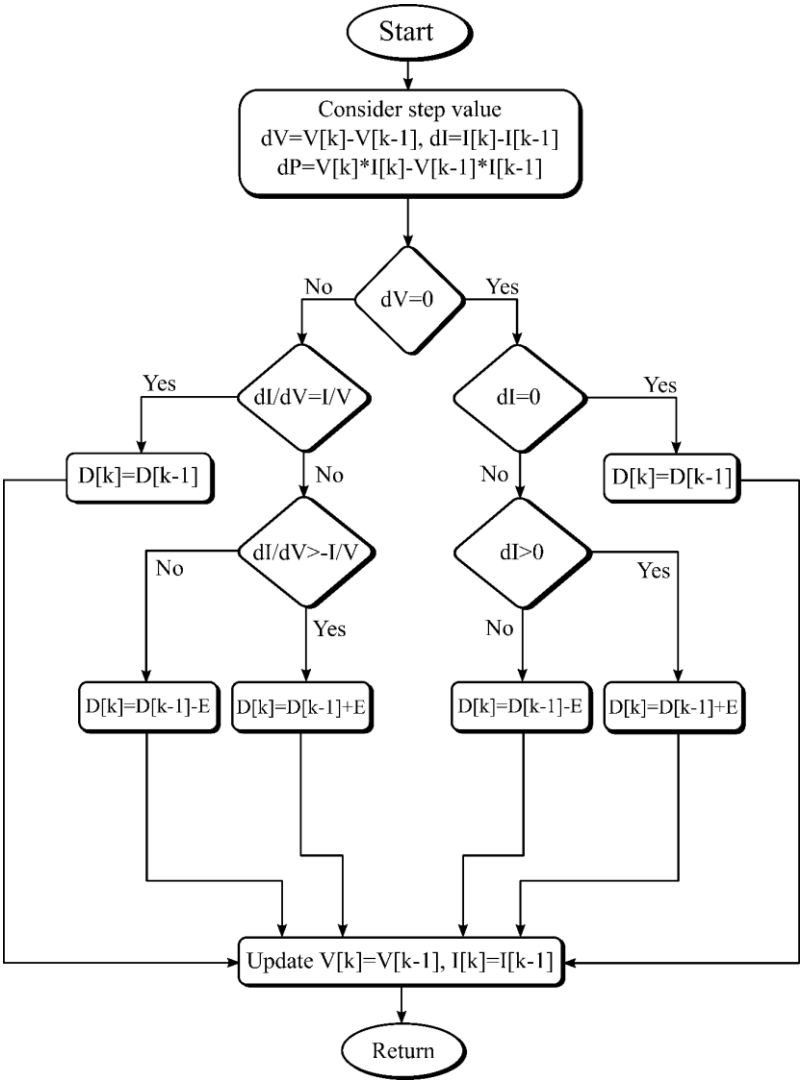

Figure 3.9 Flow chart for IC based MPPT algorithm [S.y].

Hence, the PV array terminal voltage can be adjusted relative to the MPP voltage by measuring the incremental and instantaneous array conductance's (dI/dV and I/V, respectively) and making use of equations (3.5-3.7). Fig .3.9 represents the complete operation of the incremental conductance algorithm. In this algorithm the incremental changes are represented as the difference between present values $I(k)$,$V(k)$ and the corresponding values stored at the end of the preceding cycle, $I(k-1)$ and $V(k-1)$ i.e. $dI = I(k) - I(k1)$ and $dV = V(k) - V(k-1)$ [1]. In the algorithm, mainly the search is carried out by comparing dI/dV against $-I/V$. The array terminal voltage will be shifted towards MPP voltage by adjusting the control reference signal D based on this search [1]. At the MPP, $dI/dV = -I/V$, no control action is needed, therefore the adjustment stage will be by passed and the algorithm will update the stored parameters at the end of the cycle as usual [8]. Two other checks are included in the algorithm to detect

whether a control action is required when the array was operating at the MPP in the preceding cycle ($dV = 0$); in this case the change in the atmospheric conditions is detected using ($dI \neq 0$) [9]. Now the control signal D, adjustment will depend on whether dI is positive or negative, as shown in the flow chart. When the above incremental Conductance algorithm was tested and it is observed that the condition $dP/dV = 0$ (or $dI/dV = -I/V$) seldom occurred because of the approximation made in the calculation of dI and dV [1]. However, this condition can be detected by allowing a small marginal error (E) in the above comparisons, i.e. $dP/dV = \pm E$ and E depends on MPPT Sensitivity required.

Simulink model for the PV array

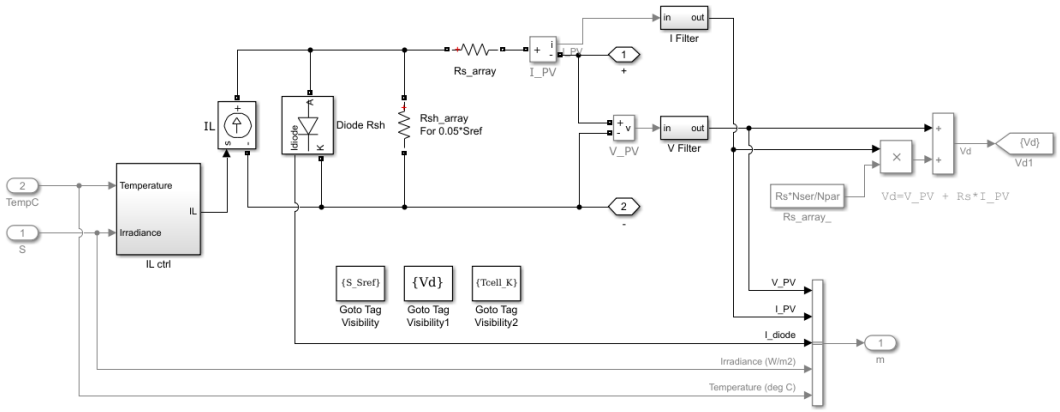

Figure 3.10 Simulink model for a PV array [S.y].

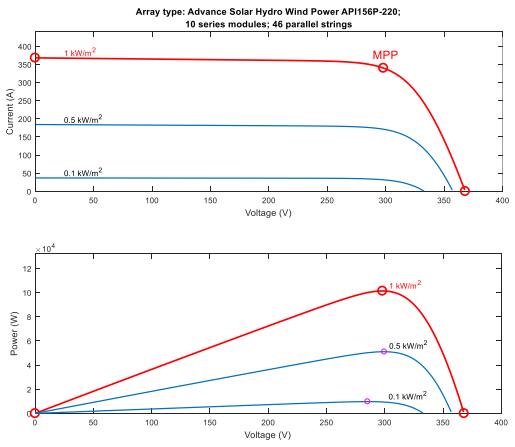

Figure 3.11 *I-V* & *P-V* curves of a PV array for different irradiance values [S.y].

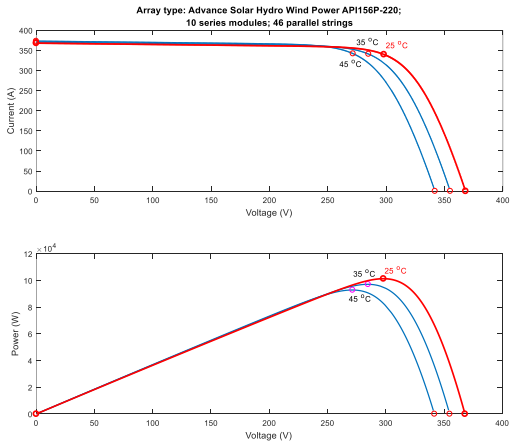

Figure 3.12 *I-V* & *P-V* curves of a PV array for different values of temperature [S.y].

The PV array simulation to plot the I-V & P-V curves can be seen in Fig. 3.10, Table. 3.1 lists the array specifications.

Table 3.1 PV array specifications.

Advance Solar Hydro Wind Power API156P-220	
Parameter	Value
Parallel strings	46
Series connected modules per string	10
Open circuit voltage V_{oc} (V)	36.8
Short circuit current I_{sc} (A)	8
Voltage at maximum power point V_{mp} (V)	29.8
Current at maximum power point I_{mpp} (A)	7.39

The *P-V* & *I-V* curves of the PV array for diverse values of irradiance are shown in Fig. 3.11 & Fig. 3.12. It is clear that with increase in solar irradiance there is a minor decrement in V_{oc} and a substantial increment in I_{sc}, as a consequence maximum power is achieved.

MATLAB/Simulink demonstration of the PV array connected to the grid through a conversion chain comprising of a boost converter controlled by the MPPT controller, a 5 level flying capacitor NPC inverter and an LCL filter is given below in the Fig. 3.13. In this work simulation was carried for a 100kW PV array. Simulation is carried out for different cases and results are presented. In all the cases temperature is assumed as a constant value which is 25°C.

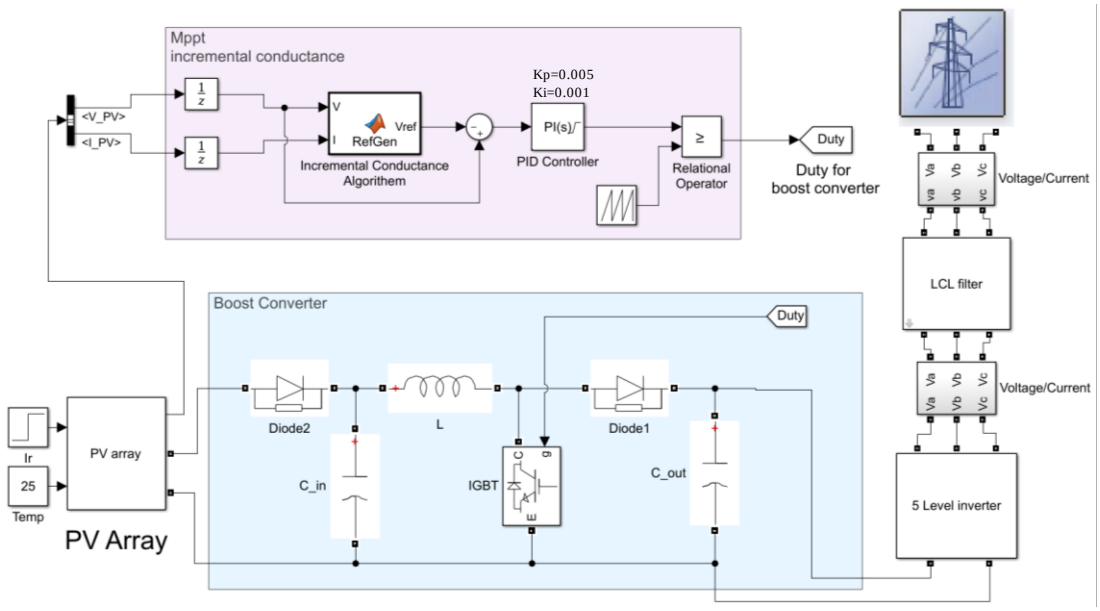

Figure 3.13 Simulation diagram of the PV system conversion chain connected to the grid highlighting the principle of the IC MPPT [S.y].

Case 1: with the MPPT

The irradiance is taken 1000W/m2 up to 0.2sec after that it reduced to 500W/m^2 until 0.34sec then it is raise again to 1000W/m2 as shown in Fig. 3.13. The MPPT controller adjusts the duty ratio of the converter, hence the panel delivers maximum power to the load.

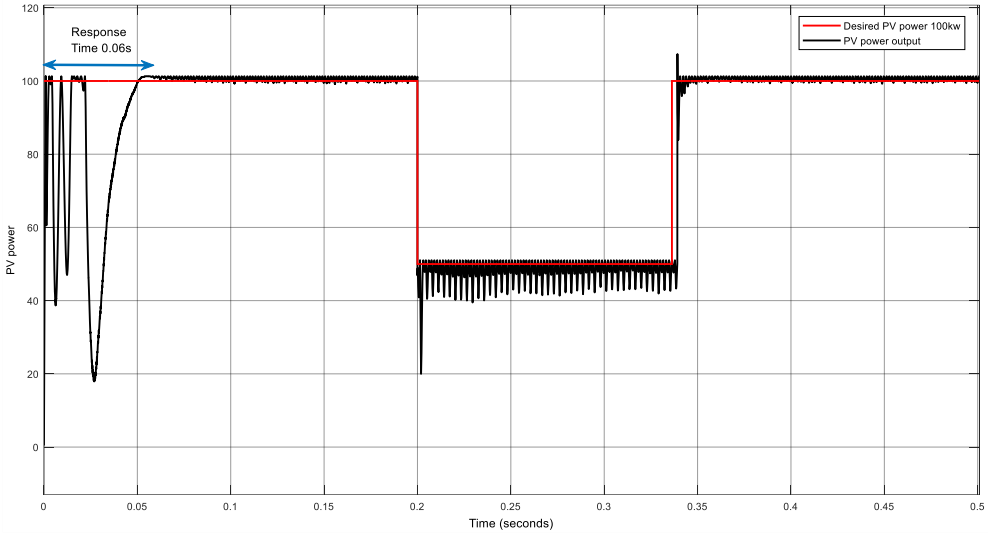

Figure 3.14 Power delivered from the solar panel with incremental conductance MPPT [S.y].

Case 2: without the MPPT

In this case solar insolation is considered as 1000W/m^2 which is shown in Fig. 3.15. PV panel Power output is different for different load resistance values as a result maximum power isn't attained.

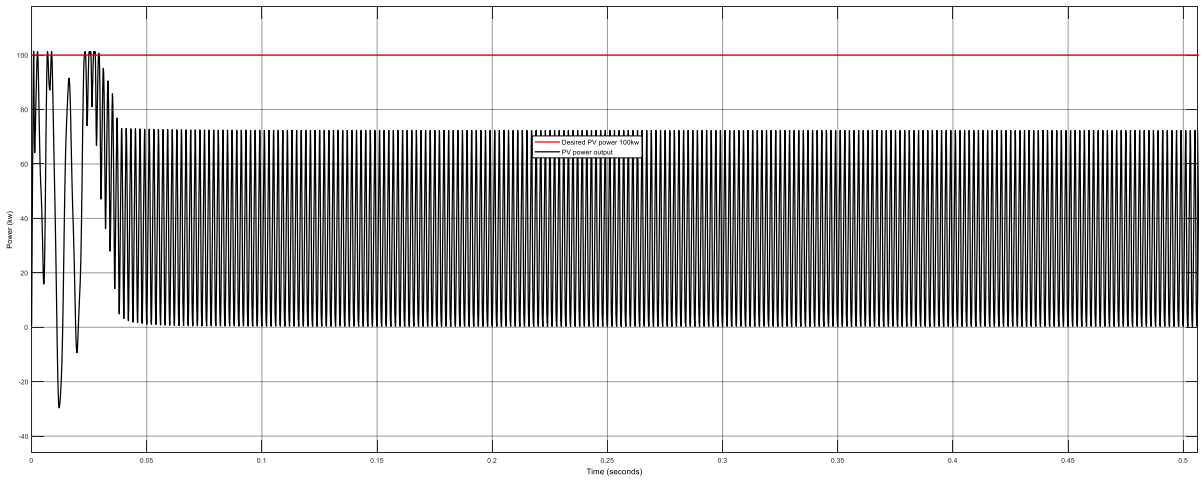

Figure 3.15 Power delivered from the solar panel without MPPT [S.y].

4. Decoupled PQ control applied to PV system connected to the grid

Decoupled PQ control (also called decoupled Watt-Var control) has been widely applied to conventional grid connected PV system. Remember that the DC continuous part of the system (PVG, Boost and MPPT) will not be studied here. We are therefore going to study only the AC alternative part which constitutes the heart of our work. In this case, the system is composed of an NPC multilevel inverter whose input voltage V_{dc} from the PV generator, an LCL filter and the electrical grid characterized by its impedance, frequency and V_{RMS} voltage. The diagram of this PQ control (in closed loop) is illustrated in Fig. 3.16.

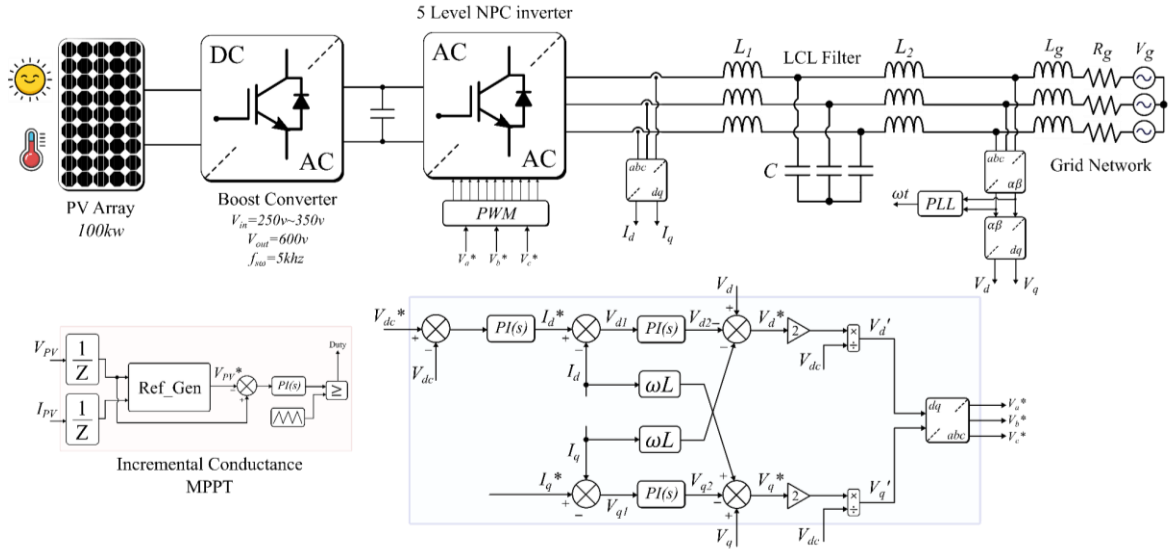

Figure 3.16 PQ control strategy applied to the PV system connected to the grid [S.y].

In a grid connected photovoltaic system, dynamic control strategy is essential to use the solar energy efficiently as well as for an energy optimization. This section of the chapter presents a decoupled control of grid connected PV system using Proportional–Integral (PI) controller. In the proposed system, closed loop high gain DC-DC converter is also employed to meet the regulated DC link voltage at the inverter input. The decoupled control strategy allows independent control of the real power (P) and the reactive power (Q) according to the power generated by photovoltaic systems and the power consumed by the utility grid [10].

4.1 The decoupling and compensation operation

In order to separately control the direct I_d and quadrature I_q component of the current and therefore the active power (P) and the reactive power (Q), we need to eliminate the coupling terms ($L\omega I_q$ and $L\omega I_d$) and compensate for the network voltage components (V_d and V_q).

So we pose:

$$\begin{cases} V_d' = V_{d2} - L\omega I_q + V_d \\ V_q' = V_{q2} + L\omega I_d + V_q \end{cases} \qquad \text{(Eq.3.8)}$$

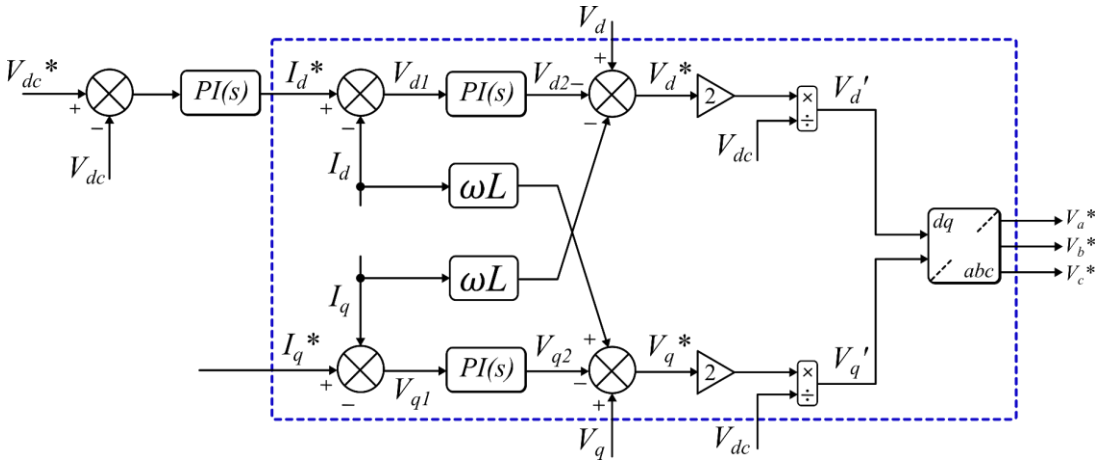

Figure 3.17 PQ control decoupling and compensation operation [S.y].

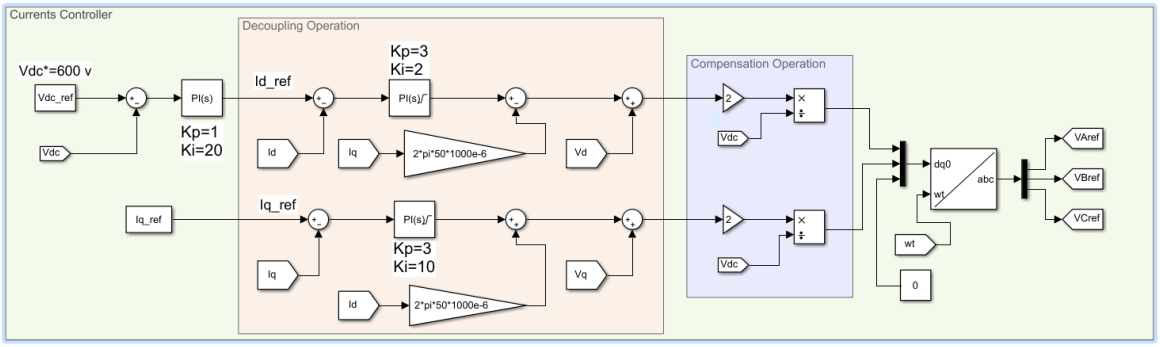

Figure 3.18 Simulation model of the decoupling and compensation operation [S.y].

The two regulators (PI) compare the reference currents (I_d* and I_q*) with the output currents of the inverter (I_d and I_q) in order to make the necessary corrections to obtain a static error. The angular frequency $\omega = 2\pi.50$, and the inductance is chosen $L = 1000 \times 10^{-6} \mu H$. The values for Kp & Ki are chosen by manually tuning the controllers.

4.2 Phase locked loop (PLL)

The basic idea of phase locking is to evaluate the difference between phase angle of the input signal and generated output signal [11]. The phase difference is usually estimated by a phase detector (which is usually a multiplier or comparator), Voltage-Controlled Oscillator (VCO) and loop controller or a Low Pass Filter (LPF). The phase angle difference between of the input signal and output signal is measured by the Phase Detector and also provides a proper error signal. To generate the output signal, the LPF output signal drives the Voltage-Controlled Oscillator (VCO). The VCO provides a measure of variations of the phase and generates a signal whose frequency is equal to its input signal [12]. The deviation of the error signal from zero is because of any change in the phase angle (or frequency) of the input signal [13]. In order to utilize renewable energy such as wind and solar energy, three-phase grid-tied inverters are widely installed in micro-grids. Using impedance based method; the stability issue caused by grid-tied inverters can be studied.

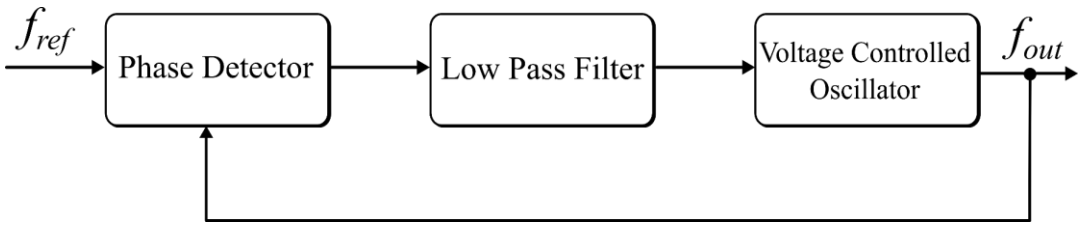

Figure 3.18 Phase Locked Loop Structure [S.y].

Phase-Locked Loop (PLL) control subsystem tracks the grid's frequency and phase angle. Hence, accurate and fast-responding PLL's for controlling of parameters are required. Ripple noise appearing in the estimated frequency is reduced or eliminated without the use of low-pass filters [11].

5. Conclusion

In this chapter we gave a general overview of the main control strategies applied to our simulation model. Firstly, we started with the multi-level inverter's modulation technique as we explained the generation of the pulses, through the comparison between a reference wave and a carrier wave to obtain the control signals for the switches of the inverter. We also showed the most common modulation strategies like APOD, POD, PD, VFC. Secondly, Application of DC-DC converter (buck converter) along with IC based MPPT is used for tracking maximum power from the solar panel. IC algorithm is tested for different cases i.e. fixed and variable irradiance levels as well as for the case of not using the

MPP tracking. From the results it is observed that the incremental conductance algorithm gives good performance for all cases, even under load variations. And lastly, we presented a decoupled PQ control method for the AC side of the system, the simulation results and discussions are presented in the last chapter of this thesis.

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Simulation results and discussions

Chapter outline

1. Introduction

In this chapter, we will work on the realization of a simulation setup for a 100kw grid connected PV system consisting of a DC side composed of a PV array and a controlled boost converter, and an AC side composed of an NPC structure multi-level inverter (5 level), an LCL filter and the distribution network. This setup is made possible using the Matlab Simulink environment to obtain the output voltages and currents.

2. Description of the simulation model

The PV array is composed of 46 parallel strings and 10 series connected modules. Which produces 100kw under the irradiance value of 1000w/m^2 and with a constant temperature value of 25°C. The PV array is connected to a boost converter, the DC side of the system is controlled with the incremental conductance MPPT, by adjusting the actual operating voltage of the array according to the voltage corresponding to maximum power. The AC side of the system we have three components, a 5 level NPC structure inverter, an LCL filter and the distribution network. The control signals for the inverter switches are obtained using the SPWM modulation technique.

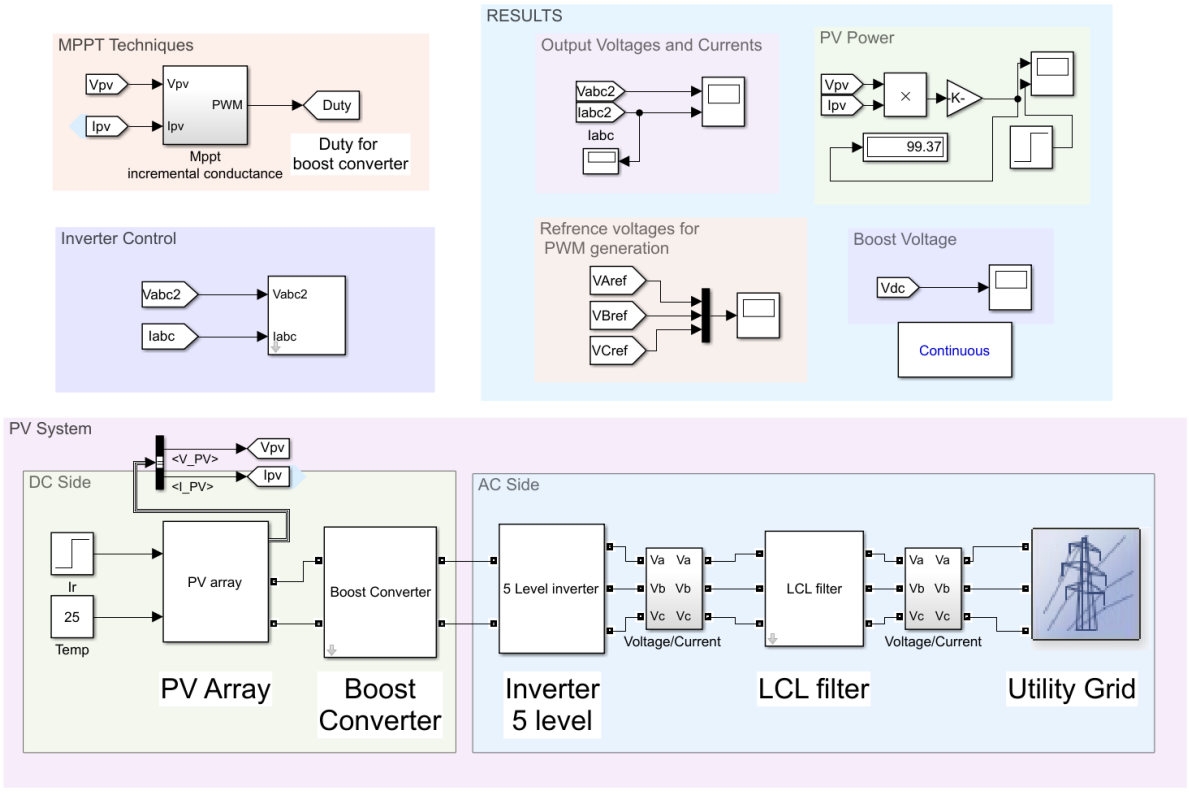

Figure 4.1 Matlab/Simulink model of the grid Connected PV system [S.y].

Table 4.1 Simulation parameters of the constituents of the grid connected PV system.

PV Array Parameters	
Parallel strings	46
Series connected modules per string	10
Open circuit voltage V_{oc} (V)	36.8
Short circuit current I_{sc} (A)	8
Voltage at maximum power point V_{mpp} (V)	29.8
Current at maximum power point I_{mpp} (A)	7.39
Boost Converter Parameters	
Input voltage (v)	250~350
Output voltage (v)	600
Input capacitor C_{in} (μF)	1000×10^{-6}
The inductance L (μH)	1.45×10^{-3}
Output capacitor C_{out} (μF)	3227×10^{-6}
Switching frequency f_{sw}	5 kHZ
Inverter Parameters	
Switching frequency f_{sw} (of the carrier wave form)	10 kHZ
LCL Filter Parameters	
Value of the input inductance L_1 (μH)	500×10^{-6}
Value of the capacitor C (μF)	100×10^{-6}
Value of the output inductance L_2 (μH)	500×10^{-6}

Note: The value for the LCL filter parameters were obtained with the process explained in chapter 2 (Electrical design of the LCL filter).

3. Simulation results

3.1 DC side

The figure below illustrates the measurements of the PV array, we've applied a constant irradiance value of 1000w/m² and a constant temperature value of 25°C.

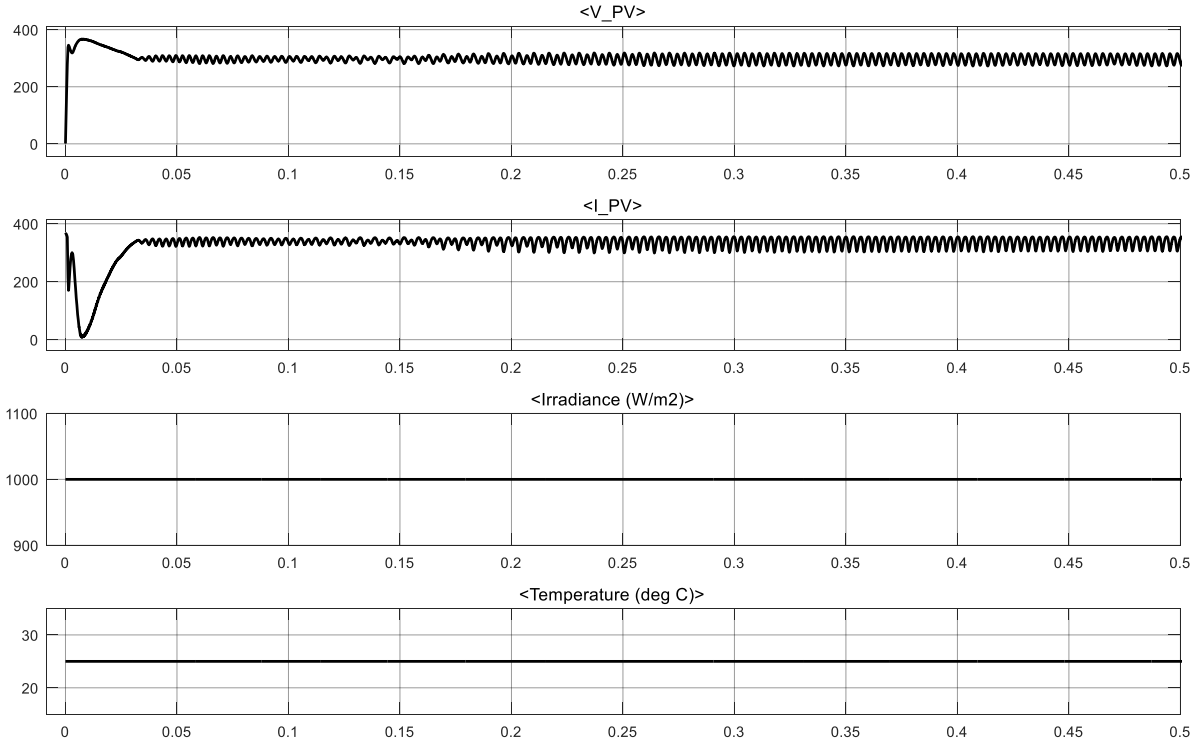

Figure 4.2 PV array measurements [S.y].

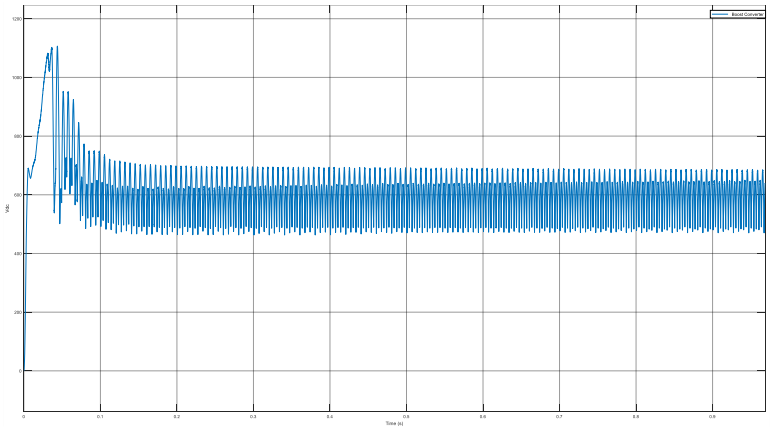

Figure 4.3 Output voltage of the boost converter V_{dc} [S.y].

Fig. 4.3 represents the voltage at the output of the boost converter V_{dc}, by including V_{dc} in the currents control loop (Chapter 3, Fig. 3.17), the controller adjusts the voltage to the desired value.

3.2 AC side

Fig. 4.4 represents the output reference voltages from the system controller, these reference voltages are compared with the carrier's wave forms to generate the control signals for the switches of the inverter.

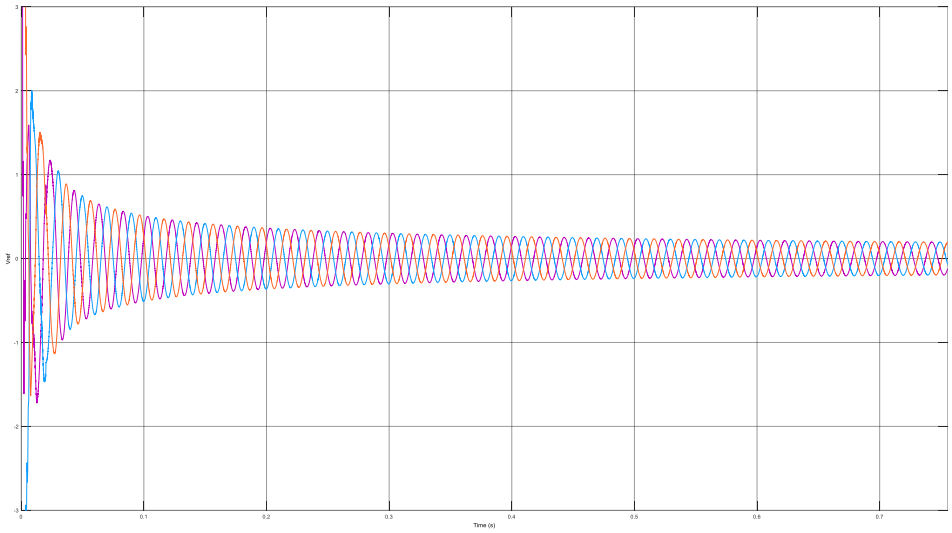

Figure 4.4 Reference voltages for PWM generation [S.y].

Fig. 4.5 shows the output voltages and currents on the grid side, with a THD level of 3.13% which comply with IEEE standards (5% THD level).

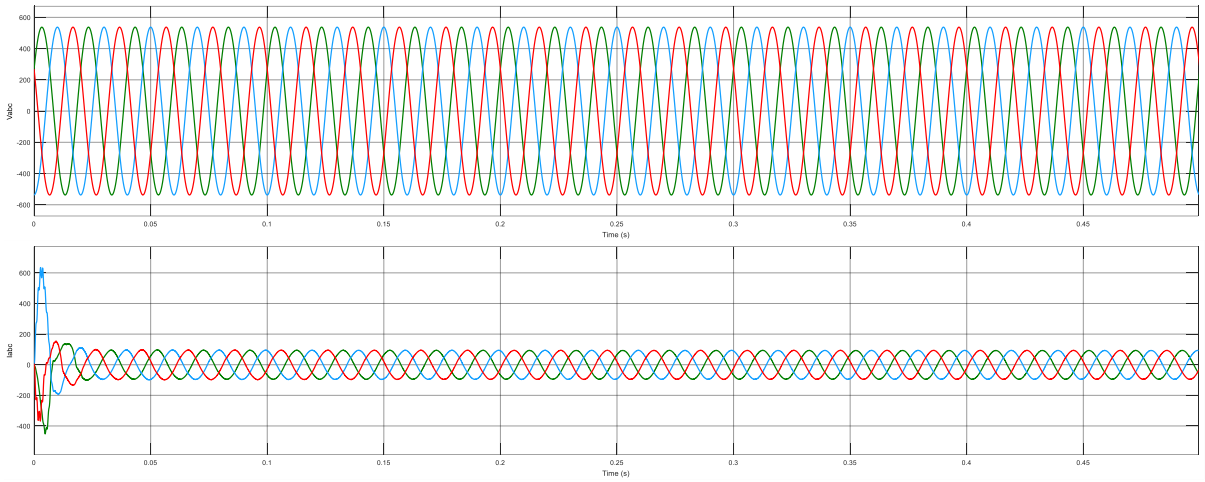

Figure 4.5 Output voltages and currents on the grid side [S.y].

In the the figure below, we ran the FFT analysis of the output currents of one phase on the grid side.

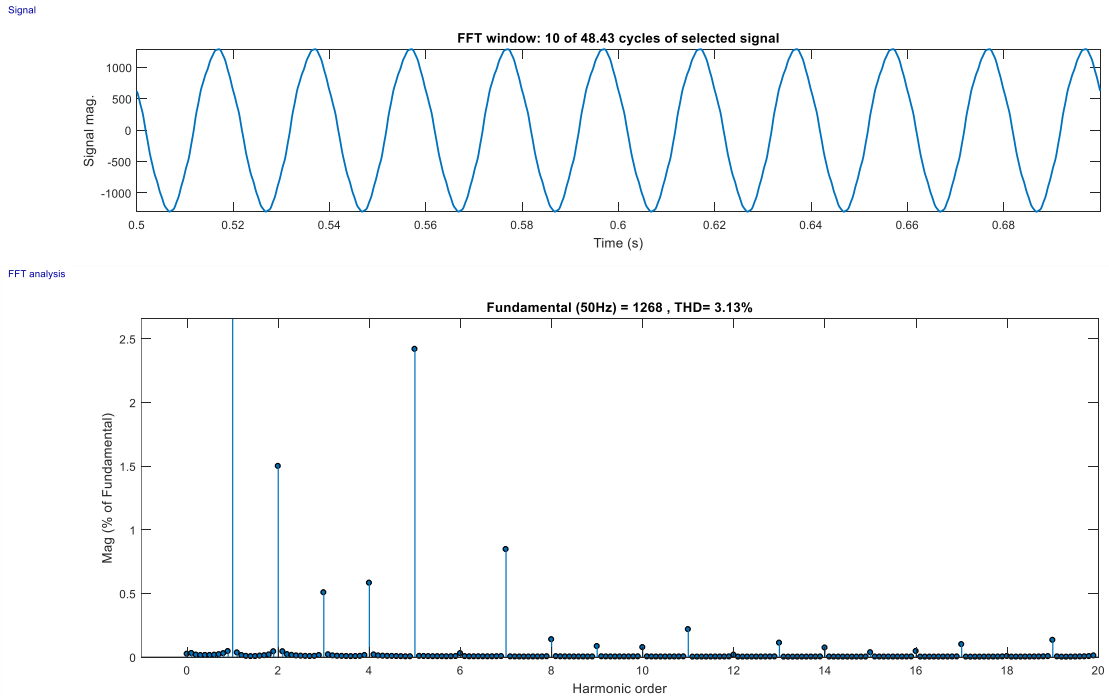

Figure 4.6 FFT analysis of the output currents on the grid side [S.y].

4. Conclusion

In this last part of the thesis, we started with a description of the final simulation model with the parameters table. Furthermore, we presented the simulation results for both the DC side and the AC side of the system with emphasis to the quality of the voltage and current wave forms injected into the distribution network by running the FFT analysis for the currents on the grid side, we managed to obtain a THD level of 3.13% which complies with IEEE standards.

General conclusion

In the first part of this thesis we gave a general system structure and the different architectures of the PV systems connected to the grid, we also gave an overview to the constituents of the grid connected PV system. In particular, the basics of the solar cell and we reviewed the different topologies of static converters especially highlighting the multilevel concept and multilevel conversion history and showed the advantages and disadvantages of each element. Finally, we closed the chapter with an overview to passive filters to which our system will be connected to eliminate certain high frequency harmonics in order to compline with the standard relating to network harmonics compatibility and grid requirements.

In the second part, a three-phase mathematical inverter model with NPC structure has been established. Then, we presented the major multi-level inverter control modulation strategy vector pulse width (SVPWM), selective harmonic elimination and sinusoidal PWM. Furthermore, Inappropriate LCL-Filter design can result in high voltage attenuation at the inverter output, resonances and oscillations can increase THD, power system instability and slow dynamic response. The LCL filter reduces ripple current and voltage at the inverter output, allowing to meet the quality standards of energy. The LCL filter also enables the inverter to be tied to the grid, thereby enhancing the power system performance.

And in the third part, we started with the multi-level inverter's modulation technique as we explained the generation of the pulses, through the comparison between a reference wave and a carrier wave to obtain the control signals for the switches of the inverter. We also showed the most common modulation strategies like APOD, POD, PD, VFC. Secondly, Application of DC-DC converter (buck converter) along with IC based MPPT is used for tracking maximum power from the solar panel. IC algorithm is tested for different cases i.e. fixed and variable irradiance levels as well as for the case of not using the MPP tracking. From the results it is observed that the incremental conductance algorithm gives good performance for all cases, even under load variations. And lastly, we presented a decoupled PQ control method for the AC side of the system.

In the last part of the thesis we presented the simulation results of the 100kv grid connected PV system.

the results obtained after several simulation tests under MATLAB, show us the efficiency of the sinusoidal PWM control algorithm, and the performance of the incremental conductance MPP used.